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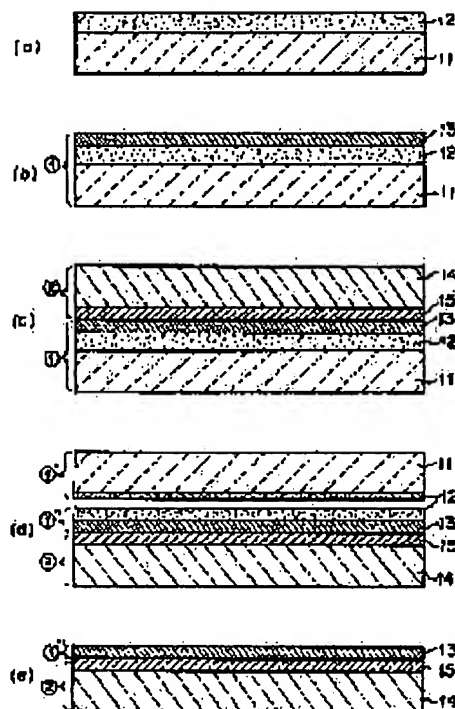
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(54) MANUFACTURE OF SEMICONDUCTOR SUBSTRATE

(57)Abstract:

PURPOSE: To remarkably lessen the defects in the single crystalline layer on an insulator by sticking a second substrate onto the nonporous single crystalline semiconductor layer made on the porous layer of a first substrate, and then, separating these two substrate at the porous layer, and then, removing the second substrate and the porous layer on the first substrate.

CONSTITUTION: The surface layer of an Si single crystalline substrate 11 is made porous 12, and a nonporous single crystalline Si layer 13 is made hereon. Next, another Si supporting substrate 14 and the single crystalline Si layer 13 are stuck fast to each other through an insulating layer 15 at high temperature, and then those are stuck together by anode junction, pressurization, or heat treatment, or these combination. Next, the boards are separated at the porous Si layer 12. Furthermore, the porous Si layer 12 is removed selectively. That is, the



single crystallized Si layer 13 in film shape is left on the insulating substrate 15+14 by etching only the porous Si layer 12 by electroless wet chemical etching. Alternatively, with the single crystalline Si layer 13 as a polishing stopper, the porous Si layer 12 is removed by selective polishing.

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CLAIMS

[Claim(s)]

[Claim 1] The process which forms a nonvesicular single crystal half conductor layer on said porous layer of the 1st base which has a porous layer, The process which sticks said nonvesicular single crystal half conductor layer with the 2nd base, the process which sticks and separates said constituted base in said porous layer, The production approach of the semi-conductor substrate characterized by having the process which removes the porous layer allotted on said 2nd separated base, and the process which removes the porous layer which constitutes said 1st separated base.

[Claim 2] The process which forms a nonvesicular single crystal half conductor layer on said porous layer of the 1st base which has a porous layer, The process which sticks said nonvesicular single crystal half conductor layer through the 2nd base and insulating layer, The production approach of the semi-conductor substrate characterized by having the process which sticks and separates said constituted base in said porous layer, the process which removes the porous layer allotted on said 2nd separated base, and the process which removes the porous layer which constitutes said 1st separated base.

[Claim 3] Said porous layer is the production approach of claim 1 constituted using silicon, or a semi-conductor substrate according to claim 2.

[Claim 4] The production approach of claim 1 which performs the process after said lamination process as the 1st base which newly forms a porous layer in the base which removes the porous layer which constitutes said 1st separated base, and is obtained, and has said porous layer for this in it, or a semi-conductor substrate according to claim 2.

[Claim 5] Said nonvesicular single crystal half conductor layer is the production approach of claim 1 which is Si layer, or a semi-conductor substrate given in 2.

[Claim 6] Said nonvesicular single crystal half conductor layer is the production approach of claim 1 which is a compound semiconductor layer, or a semi-conductor substrate given in 2.

[Claim 7] Said 1st base is the production approach of claim 1 constituted using Si, or a semi-conductor substrate given in 2.

[Claim 8] Said 2nd base is the production approach of claim 1 which is a light transmission nature base, or a semi-conductor substrate given in 2.

[Claim 9] Removal of said porous layer is the production approach of claim 1 made using etching, or a semi-conductor substrate given in 2.

[Claim 10] Removal of said porous layer is the production approach of claim 1 made by grinding alternatively said nonvesicular single crystal half conductor layer for said porous layer as a stopper, or a semi-conductor substrate given in 2.

[Claim 11] The separation in said porous layer is the production approach of claim 1 performed by at least one or more approaches of pressurizing in the perpendicular direction to the lamination side of the stuck base, pulling in the direction perpendicular to said field, and applying to this lamination side-shearing stress **, or a semi-conductor substrate given in 2.

[Claim 12] Said insulating layer is the production approach of the semi-conductor substrate according to claim 2 formed at least in one side on the front face of said 2nd base on said nonvesicular single crystal

layer.

[Claim 13] Said insulating layer is the thermal oxidation film and deposition SiO₂. The film and deposition Si₃N₄ The production approach of the semi-conductor substrate according to claim 12 chosen from film.

[Claim 14] Said lamination process is the production approach of the semi-conductor substrate according to claim 1 or 2 performed by anode plate junction, pressurization, heat treatment, or the approach chosen from such combination.

[Claim 15] Said porous layer is the production approach of the semi-conductor substrate according to claim 1 or 2 formed using anodization.

[Claim 16] Said anodization is the production approach of the semi-conductor substrate according to claim 15 performed in HF solution.

[Claim 17] The separation in said porous layer is the production approach of claim 1 performed by impressing wave energy to this porous layer, or a semi-conductor substrate given in 2.

[Claim 18] The separation in said porous layer is the production approach of claim 1 performed by inserting the member for exfoliation from this porous layer side face, or a semi-conductor substrate given in 2.

[Claim 19] The separation in said porous layer is the production approach of claim 1 performed by the expansion energy of the matter into which this porous layer was infiltrated, or a semi-conductor substrate given in 2.

[Claim 20] The separation in said porous layer is the production approach of claim 1 performed by the selective etching to this porous layer of a wafer side face, or a semi-conductor substrate given in 2.

[Claim 21] The porosity of said porous layer is the production approach of claim 1 in 10 - 80% of range, or a semi-conductor substrate given in 2.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to the production approach of a semi-conductor substrate. Furthermore, it is related with the production approach of the production approach of dielectric separation or the single crystal semiconductor of an insulating lifter, and the single crystal compound semiconductor on a half-dynamic body substrate, the electron device further created by the single crystal half conductor layer, and the semi-conductor substrate suitable for an integrated circuit in detail.

[0002]

[Description of the Prior Art] Formation of the single crystal Si semi-conductor layer of an insulating lifter is silicon. ON It was widely known as an insulator (SOI) technique, and in the bulk Si substrate which produces the usual Si integrated circuit, since the device using a SOI technique has many dominance points which cannot reach, many researches have accomplished. That is, the possibility of the perfect depletion mold field-effect transistor by the formation of 6. thin film which can prevent 5. latch rise which 3. stray capacity 1. dielectric separation excels [stray capacity] in the possibility of high integration and 2. opposite radiation resistance easily is reduced, and can skip the possibility of improvement in the speed and 4. well process by using a SOI technique, and the dominance point of ** are acquired.

[0003] In order to realize many advantages on a device property which was described above, it has inquired about the formation approach of SOI structure over the past dozens of years. These contents are summarized in the following reference.

[0004] Special Issue: "Single-crystal silicon on non-single-crystal insulators"; edited by G.W. Cullen and Journal of Crystal Growth and volume 63, no3, and pp429-590(1983). -- in ancient times again SOS (silicon ON sapphire) which is made to carry out hetero epitaxy of the Si, and forms it by CVD (chemistry gaseous-phase method) on single crystal silicon on sapphire is known, and a success temporary as a SOI technique which matured most is stored. A fraction The breadth of the application is barred by the grid mismatching of Si layer and a substrate silicon-on-sapphire interface by the expensive rank of a substrate, and the delay to large-area-izing rather than mixing to a lot of crystal defects and Si layer of the aluminum from silicon on sapphire, and anything. The attempt in which SOI structure will be realized without using silicon on sapphire is performed comparatively at recent years. This attempt is divided roughly into the following two.

- [0005] 1. Open an aperture for Si single crystal substrate after scaling, make Si substrate express partially, carry out epitaxial growth to a longitudinal direction by considering the part as seed, and it is SiO₂. Si single crystal layer is formed upwards. (In this case, SiO₂. It is accompanied by deposition of Si layer upwards)
2. Use the Si single crystal substrate itself as a barrier layer, and it is SiO₂ to the lower part. It forms. (This approach is not accompanied by deposition of Si layer.) The device on a compound semiconductor has the high engine performance which is not obtained, for example, a high speed, luminescence, etc. by Si again. Most of these devices carries out epitaxial growth on compound semiconductor substrates,

such as GaAs, and current is made in it.

[0006] However, a compound semiconductor substrate is expensive, a mechanical strength is low, and a large area wafer has which trouble with difficult creation.

[0007] From such a thing, it is cheap, and a mechanical strength is also high and the attempt which carries out heteroepitaxial growth of the compound semiconductor on Si wafer which can produce a large area wafer is made.

[0008]

[Problem(s) to be Solved by the Invention] As a means to realize the above 1, the approach and amorphous Si to which longitudinal direction epitaxial growth of the single crystal layer Si is carried out are directly deposited by CVD. The approach, amorphous substance which carry out solid phase longitudinal direction epitaxial growth by heat treatment or a polycrystal Si layer -- energy beams, such as an electron ray and laser light, -- converging -- irradiating -- melting recrystallization -- a single crystal layer -- SiO₂ the approach of making it growing up upwards -- and The approach (Zone Melting Recrystallization) of scanning a melting field to band-like at a cylindrical heater is learned. Although there are merits and demerits in these approaches, respectively, it has left the great problem to the controllability, productivity, homogeneity, and quality, and there is nothing that was still put in practical use industrially. For example, in order to form a flat thin film, sacrifice oxidation is needed and the crystallinity of a CVD method is bad in a solid phase grown method. Moreover, by the beam annealing method, a problem is in the processing time by convergence beam scan, and controllabilities, such as lap condition of a beam, and focus control. Among these, Zone Melting Although the Recrystallization method has matured most and the comparatively large-scale integrated circuit is also made as an experiment, remaining and creating a minority carrier device does not still have many crystal defects, such as a subgrain boundary, very much.

[0009] In the approach of not using Si substrate which is the approach of the above 2 as a seed of epitaxial growth, four kinds of approaches as follows are mentioned.

[0010] 1. Form an oxide film in Si single crystal substrate with which anisotropic etching of the slot on the V type was carried out to the front face, and form Si single crystal field as for which was surrounded by the V groove and dielectric separation was carried out by polish on the thick polycrystal Si layer from the rear face of Si substrate after depositing a polycrystal Si layer thickly on this oxide film degree it is the same as Si substrate. In this technique, although crystallinity is good, a problem is in the process which deposits the hundreds of microns polycrystal Si thickly, and the process which leaves only Si barrier layer which ground the single crystal Si substrate from the rear face, and was separated from the point of a controllability and productivity.

[0011] 2. It is SiO₂ by the ion implantation of oxygen in Si single crystal substrate called SIMOX (SIMOX: Separation by ion implanted oxygen). It is the approach of forming a layer, and since Si process and adjustment are good, they are current but the technique of having matured. However, SiO₂ It is oxygen ion in order to form a layer 10¹⁸ ions/cm² Although it is necessary to also pour in the above, the impregnation time amount is huge, it cannot say that productivity is high and wafer cost is high. Furthermore, many crystal defects remain, are seen industrially and it has not resulted in sufficient quality which can produce a minority carrier device.

[0012] 3. How to form SOI structure according to dielectric separation by oxidation of Porosity Si. This approach is the approach of carrying out dielectric separation of the N type Si island by accelerating oxidation, after porosity-izing only a P type Si substrate by the anodization method in HF solution so that an N type Si layer may be formed in a P type Si single crystal substrate front face at island shape by the proton ion implantation, (J.Crystal Growth besides Imai, vol 63,547) (1983), or epitaxial growth and patterning and Si island may be surrounded from a front face. By this approach, Si field separated is determined before the device process, and there is a trouble that the degree of freedom of a device design may be restricted.

[0013] Moreover, apart from the formation approach of the above conventional SOI, the approach of using heat treatment or adhesives for another Si single crystal substrate which oxidized Si single crystal substrate thermally, and forming lamination and SOI structure is capturing the spotlight in recent years.

This approach needs to thin-film-ize the barrier layer for a device to homogeneity. That is, it is necessary to thin-film-ize Si single crystal substrate with a thickness of hundreds of microns less than [micron order or it]. There are two kinds of approaches in this thin film-ization as follows.

[0014] 1. It is difficult to thin-film-ize to homogeneity in polish of the thin-film-izing 1 by the thin film-ized 2. selective etching by polish. Especially as for submicron thin film-ization, dispersion also becomes dozens of% and this equalization poses a big problem. If diameter-ization of macrostomia of a wafer furthermore progresses, whenever [the / difficult] will just increase.

[0015] Moreover, although etching of 2 is confirmed to uniform thin-film-izing - At most 102 - ion implantation with the bad front-face nature after - etching whose selection ratio is not enough, since the epitaxial growth or heteroepitaxial growth on a high concentration B dope Si layer is used, there are troubles, like the crystallinity of a SOI layer is bad (C. -- Harendt, et.al., and J.Elect.Mater.Vol.20,267 (1991) --) H. Baumgart, et.al., Extended Abstract of ECS 1st International Symposium of Wafer Bonding pp-733 (1991), C. E.Hunt, Extended Abstract of ECS 1st International Symposium of Wafer Bonding, pp-696 (1991).

[0016] Furthermore the semi-conductor substrate using lamination surely needs two wafers, and among those, most will almost be vainly removed by polish, etching, etc., and one sheet will be thrown away, and will waste the resource of the limited earth.

[0017] Therefore, in SOI by lamination, many troubles exist in the controllability and a homogeneous pan by the present approach at economical efficiency.

[0018] Moreover, on the light transmission nature substrate represented by glass, generally, from the disorderly nature of the crystal structure, reflecting the disorderly nature of a substrate, the deposited thin film Si layer is not good, and turns into only a polycrystal layer in an amorphous substance, and a highly efficient device cannot be produced. It gets down from it according to the crystal structure of a substrate being amorphous, and even if it deposits Si layer, a good single crystal layer is not only obtained.

[0019] By the way, a light transmission nature substrate constitutes the contact sensor and projection mold liquid crystal image display device which are an optical photo detector, and also is important. and the pixel (picture element) of a sensor or a display -- more -- much more -- densification and high-resolution-izing -- in order to carry out high elaboration, a highly efficient driver element is needed. Consequently, it is necessary to be produced using the single crystal layer which has the crystallinity which was excellent also as a component prepared on the light transmission nature substrate.

[0020] Therefore, it is difficult to produce the crystal structure with many the defect, therefore the driver element which had sufficient engine performance to be required from now on or it was required in amorphous Si or Polycrystal Si.

[0021] As stated in the top, the substrate of a compound semiconductor is indispensable to device production of a compound semiconductor. However, the substrate of a compound semiconductor is expensive and, moreover, large-area-izing is very difficult for it.

[0022] Furthermore, although to carry out epitaxial growth of the compound semiconductors, such as GaAs, on Si substrate is tried, it is very difficult for the growth film to have bad crystallinity and to apply to a device by the difference in a lattice constant or a coefficient of thermal expansion.

[0023] Moreover, although to carry out epitaxial growth of the compound semiconductor on Porosity Si is tried in order to ease the misfit of a grid, the stability as a substrate under production or after producing, and dependability are missing in a device with the lowness of the thermal stability of Porosity Si, aging, etc.

[0024] Meanwhile, Takao Yonehara who is the artificer of this invention proposed the manufacture approach of the new semi-conductor member previously indicated by JP,5-21338,A in view of the technical-problem point mentioned above.

[0025] The approach indicated by the official report concerned is a thing as follows. That is, after it forms the member which allotted the nonvesicular single crystal semiconductor region on a porosity single crystal semiconductor region and a front face sticks the front face of the member which consisted of insulating matter on the front face of said nonvesicular single crystal semiconductor region, it is the

manufacture approach of the semi-conductor member characterized by removing said porosity single crystal semiconductor region by etching.

[0026] The approach concerned can solve the technical problem mentioned above, and is excellent. However, if the approach indicated by the official report concerned is developed further and improvement in the productivity of a semi-conductor substrate and low cost-ization can be attained further, the contribution to the industry concerning the technical field concerned will become very big.

[0027] [Purpose of invention] this invention aims at offering the production approach of a semi-conductor substrate of having improved further the approach indicated by the above-mentioned official report.

[0028] another purpose of this invention -- economical efficiency -- excelling -- a large area -- crossing - - homogeneity -- it leaves the semi-conductor layer or compound semiconductor barrier layer formed in the front face using the flat single crystal substrate which has the extremely excellent crystallinity, this from the one side to barrier layer is removed, and it is in offering the production approach of a semi-conductor substrate of obtaining few remarkable single crystal layers or compound semiconductor crystal layer of a defect to an insulating lifter.

[0029] Still more nearly another purpose of this invention is to propose the production approach of the semi-conductor substrate which stood high in the field of productivity, homogeneity, a controllability, and cost on the transparence substrate (light transmission nature substrate) when crystallinity obtained Si which was excellent just like the single crystal wafer, or a compound semiconductor single crystal layer.

[0030] Also in case still more nearly another purpose of this invention produces the large-scale integrated circuit of SOI structure, it is to propose the production approach of expensive SOS and the alternative ***** substrate of SIMOX.

[0031]

[Means for Solving the Problem] The production approach of the semi-conductor substrate of this invention is the thing of a configuration of lower-**(ing).

[0032] Namely, the 1st mode of the production approach of the semi-conductor substrate of this invention The process which forms a nonvesicular single crystal half conductor layer on said porous layer of the 1st base which has a porous layer, The process which sticks said nonvesicular single crystal half conductor layer with the 2nd base, the process which sticks and separates said constituted base in said porous layer, It is characterized by having the process which removes the porous layer allotted on said 2nd separated base, and the process which removes the porous layer which constitutes said 1st separated base.

[0033] The process which forms a nonvesicular single crystal half conductor layer on said porous layer of the 1st base with which the 2nd mode of this invention has a porous layer, The process which sticks said nonvesicular single crystal half conductor layer through the 2nd base and insulating layer, It is characterized by having the process which sticks and separates said constituted base in said porous layer, the process which removes the porous layer allotted on said 2nd separated base, and the process which removes the porous layer which constitutes said 1st separated base.

[0034]

[Function] In this invention, it sticks, the constituted base is separated by the porous layer, and the semi-conductor base with which the quality nonvesicular single crystal half conductor layer was allotted can be formed by removing the porous layer on the 2nd base to which the nonvesicular single crystal half conductor layer was allotted. In addition, it can stick, the constituted base can be separated by the porous layer, and the 1st base from which the porous layer was removed can be reused to semi-conductor base production by removing the porous layer which constitutes the 1st base. Thereby, improvement in the productivity of a semi-conductor base and low cost-ization can be attained further.

[0035] According to this invention, the production approach of the semi-conductor substrate which stood high in the field of productivity, homogeneity, a controllability, and cost on substrates including a transparence substrate (light transmission nature substrate) when crystallinity obtained a single crystal layer or compound semiconductor single crystal layers, such as Si which was excellent just like the

single crystal wafer, can be proposed.

[0036] Moreover, according to this invention, also in case the large-scale integrated circuit of SOI structure is produced, the production approach of expensive SOS and the alternative ***** substrate of SIMOX can be proposed.

[0037] In this invention, a base is separable into two or more through a porous layer, and after one base after separation removes residual porosity, it is usable as a semi-conductor substrate, and after removing residual porosity, it is applicable [the base of another side] to production of a semi-conductor substrate again.

[0038] In this invention, a porous layer and a nonvesicular single crystal layer are formed in both sides of a base, and after sticking another base of two sheets so that this single crystal layer may be pinched, two semi-conductor substrates are producible to coincidence by separating a base by said porous layer.

[0039] The production approach of the semi-conductor substrate of this invention is mentioned as an example, and silicon is explained below at a detail.

[0040] Although the mechanical strength of Porosity Si changes with porosit(ies), it is thought that it is weaker enough than bulk Si. For example, as long as porosity is 50%, a mechanical strength may consider the one half of bulk. That is, it compresses into a lamination wafer, and when it pulls or shearing force is applied, a porosity Si layer will be destroyed first. Moreover, if porosity is made to increase, a porous layer can be destroyed by the weaker force.

[0041] Si substrate can be made to porosity-ize by the anodization method which used HF solution. This porosity Si layer is consistency 2.33 g/cm³ of a single crystal Si. That consistency can be changed to the range of 1.1 - 0.6 g/cm³ by comparing and changing HF solution concentration to 50 - 20%. This porous layer is not formed in an N type Si layer of the following reason, but is formed only in a P type Si substrate of it. According to observation according [this porosity Si layer] to a transmission electron microscope, the hole of a diameter with an average of about 600Å is formed.

[0042] Porosity Si was discovered by Uhlir etc. in the research process of electrolytic polishing of a semi-conductor in 1956 (A. Uhlir, Bell Syst.Tech.J., vol.35,333 (1956)).

[0043] Moreover, Unagami etc. studied the lytic reaction of Si in anodization, an electron hole is required for the anodic reaction of Si in HF solution, and the reaction has reported that it is as follows (T. Unagami, J.Electrochem.Soc., vol.127,476 (1980)).

[0044] $\text{Si} + 2\text{HF} + (2-n) e^- \rightarrow \text{SiF}_2 + 2\text{H}^+ + ne^-$ $\text{SiF}_2 + 2 \text{HF} \rightarrow \text{SiF}_4 + \text{H}_2\text{SiF}_4 + 2 \text{HF} \rightarrow \text{H}_2 \text{SiF}_6$ or $\text{Si} + 4\text{HF} + (4-\lambda) e^- \rightarrow \text{SiF}_4 + 4\text{H}^+ + \lambda e^-$ $\text{SiF}_4 + 2 \text{HF} \rightarrow \text{H}_2 \text{SiF}_6$ -- here -- e^+ And e^- The electron hole and the electron are expressed, respectively. Moreover, n and lambda are the number of electron holes required in order that a Si atom may dissolve, respectively, and when $n > 2$ or the conditions which become $\lambda > 4$ are fulfilled, they suppose that Porosity Si is formed.

[0045] Although P type Si in which an electron hole exists is porosity-ized from the above thing, N type Si is not porosity-ized. The selectivity in this porosity-izing is proved [Imai /, such as Nagano,] (KImai, Solid-State Electronics, vol.24,159 (1981)). (Nagano, Nakajima, Yasuno, Onaka, Kajiwar, the Institute of Electronics and Communication Engineers technical research report, vol.79, SSD 79-9549 (1979))

[0046] However, it is important to choose the substrate which a report that it is porosity-ized also has if it is high concentration N type Si (R. P.Holmstrom and J.Y.Chi, Appl.Phys.Lett., vol.42,386 (1983)), and is not scrupulous according to P type and N type, and can realize porosity-ization.

[0047] According to observation by the transmission electron microscope, although the hole of a diameter with an average of about 600Å is formed and the consistency becomes below one half compared with a single crystal Si, single crystal nature is maintained by the porosity Si layer, and it is also possible in it to carry out epitaxial growth of the single crystal Si layer to the upper part of a porous layer. However, above 1000 degrees C, the rearrangement of an internal hole happens and the property of accelerating etching is spoiled. For this reason, low-temperature growth of molecular-beam epitaxial growth, plasma CVD, a reduced pressure CVD method, Light CVD, a bias sputtering technique, a liquid phase grown method, etc. is made suitable at the epitaxial growth of Si layer.

[0048] Moreover, since a lot of [a porous layer] openings to the interior are formed, a consistency decreases below in one half. Consequently, since surface area increases by leaps and bounds compared

with the volume, compared with the etch rate of the usual single crystal layer, it accelerates the chemical etching rate remarkably.

[0049] As shown in [example 1 of embodiment] drawing 1 (a), 1st Si single crystal substrate 11 is prepared first, the surface layer is carried out porosity-ized 12, and the nonvesicular single crystal Si layer 13 is formed on porosity Si 12 (drawing 1 (b)).

[0050] Next, as shown in drawing 1 (c), after sticking another Si support substrate 14 and single crystal Si layer 13 at a room temperature through an insulating layer 15, it sticks with anode plate junction, pressurization, heat treatments, or such combination. This combines firmly Si support substrate 14 and the single crystal layer 13 through an insulating layer 15. Or it forms an insulating layer 15 at least in one side on a single crystal Si layer and Si support substrate 14, it is stuck by the three-sheet pile on both sides of insulating sheet metal.

[0051] Next, a substrate is separated in the porosity Si layer 12 (drawing 1 (d)). Si support substrate side serves as structure like the 15/Si support substrate 14 of 13/insulating layers of porosity Si 12/single crystal Si layers.

[0052] Furthermore, porosity Si 12 is removed alternatively. The fluoric acid which is the etching reagent of usual Si, or the selection etching reagent of Porosity Si, To fluoric acid, or alcohol and mixed liquor of hydrogen peroxide solution which added either at least, Or at least one kind of the mixed liquor of alcohol and hydrogen peroxide solution which added either at least is used for buffered fluoric acid or buffered fluoric acid. Non-electrolyzed wet chemical etching of the porosity Si 12 is carried out, and on insulating substrate 15 +14, the thin-film-ized single crystal Si layer 13 is made to remain, and it forms. As the detailed explanation was carried out [above-mentioned], it is possible for the etching reagent of usual Si to also etch Porosity Si alternatively with the huge surface area of Porosity Si.

[0053] Or porosity Si 12 is removed by selection polish by using the single crystal Si layer 13 as a polish stopper.

[0054] The semi-conductor substrate obtained by this invention is shown in drawing 1 (e). The semi-conductor substrate which lamination is carried out evenly [the single crystal Si layer 13] to homogeneity, and is formed throughout a wafer on insulating substrate 15 +14 at a large area and which was obtained in this way can be suitably used, even if it sees from the point of electronic device production by which insulating separation was carried out.

[0055] 1st Si single crystal substrate 11 removes the residual porosity Si, and when ruined so that surface surface smoothness is nonpermissible, after it performs surface flattening, it is again used for it as 1st Si single crystal substrate 11.

[0056] The approach of pressurizing from the both sides of the base stuck as an approach of separating two bases in a porosity Si layer in this invention, and crushing a porous layer, and each base are lengthened on both sides, and the approach of separating both, the method of inserting a fixture to a porous layer, the method of applying the force in the direction parallel to the front face of the stuck base, the method of adding supersonic vibration to a porous layer, etc. can be adopted.

[0057] In this invention, generally the porosity (porosity) of the porosity Si layer suitable for separation is 10 - 80% of range, and is 20 - 60% of range more preferably.

[0058] As shown in [example 2 of embodiment] drawing 2 (a), 1st Si single crystal substrate 21 is prepared first, the surface layer is carried out porosity-ized 22, and the nonvesicular single crystal Si layer 23 is formed on porosity Si 22 (drawing 2 (b)).

[0059] Next, as shown in drawing 2 (c), after sticking the light transmission nature support substrate 24 and the single crystal Si layer 23 which are represented by a quartz and glass at a room temperature through an insulating layer 25, it sticks with anode plate junction, pressurization, heat treatments, or such combination. This combines firmly the light transmission nature support substrate 24 and the single crystal layer 23 through an insulating layer 25. Or it forms an insulating layer 25 at least in one side on a single crystal Si layer and the light transmission nature support substrate 24, it is stuck by the three-sheet pile on both sides of insulating sheet metal.

[0060] Next, a substrate is divided in the porosity Si layer 23 (drawing 2 (d)). A light transmission nature support substrate side serves as structure like the 25/light transmission nature support substrate 24

of 23/insulating layers of porosity Si22/single crystal Si layers.

[0061] Furthermore, porosity Si 22 is removed alternatively. The fluoric acid which is the etching reagent of usual Si, or the selection etching reagent of Porosity Si, To fluoric acid, or alcohol and mixed liquor of hydrogen peroxide solution which added either at least, Or at least one kind of the mixed liquor of alcohol and hydrogen peroxide solution which added either at least is used for buffered fluoric acid or buffered fluoric acid. Non-electrolyzed wet chemical etching of the porosity Si 22 is carried out, and on light transmission nature insulation substrate 25 +24, the thin-film-ized single crystal Si layer 23 is made to remain, and it forms. As the detailed explanation was carried out [above-mentioned], it is possible for the etching reagent of usual Si to also etch Porosity Si alternatively with the huge surface area of Porosity Si.

[0062] Or porosity Si 22 is removed by sorting polish by using the single crystal Si layer 23 as a polish stopper.

[0063] The semi-conductor substrate obtained by this invention is shown in drawing 2 (e). On light transmission nature insulation base 25 +24, evenly, lamination of the single crystal Si layer 23 is carried out to homogeneity, and it is formed throughout a wafer at a large area. In this way, the obtained semi-conductor substrate can be suitably used, even if it sees from the point of electronic device production by which insulating separation was carried out.

[0064] There may not be the insulating mediation layer 25.

[0065] 1st Si single crystal substrate 21 removes the residual porosity Si, and when ruined so that surface surface smoothness is nonpermissible, after it performs surface flattening, it can be again used for it as 1st Si single crystal substrate 21.

[0066] As shown in [example 3 of embodiment] drawing 3 (a), 1st Si single crystal substrate 31 is prepared first, the surface layer is carried out porosity-ized 32, and the nonvesicular single crystal compound semiconductor layer 33 is formed on porosity Si 32 (drawing 3 (b)).

[0067] Next, as shown in drawing 3 (c), after sticking another Si support substrate 34 and single crystal compound semiconductor layer 33 at a room temperature through an insulating layer 35, it sticks with anode plate junction, pressurization, heat treatments, or such combination. This combines firmly Si support substrate 34 and the single crystal layer 33 through an insulating layer 35. Three insulating layers 35 are stuck in piles on both sides of insulating sheet metal, or it forms at least in one side on a single crystal compound semiconductor layer and Si support substrate 34.

[0068] Next, a substrate is divided in the porosity Si layer 32 (drawing 3 (d)). Si support substrate side serves as structure like the 35/Si support substrate 34 of 33/insulating layers of porosity Si32/single crystal compound semiconductor layers.

[0069] Furthermore, porosity Si 32 is removed alternatively. Chemical etching of the porosity Si 32 is carried out using an etching reagent with the early etch rate of Si to a compound semiconductor, and on insulating substrate 35 +34, the thin-film-ized single crystal compound semiconductor layer 33 is made to remain, and it forms.

[0070] Or porosity Si 32 is removed by selection polish by using the single crystal compound semiconductor layer 33 as a polish stopper.

[0071] The semi-conductor substrate obtained by this invention is shown in drawing 3 (e). On insulating substrate 35 +34, evenly, lamination of the single crystal compound semiconductor layer 33 is carried out to homogeneity, and it is formed throughout a wafer at a large area. In this way, the obtained semi-conductor substrate can be suitably used, even if it sees as a compound semiconductor substrate from the point of electronic device production by which insulating separation was carried out further.

[0072] When using as a compound semiconductor substrate, there may not be an insulating layer 35.

[0073] 1st Si single crystal substrate 31 removes the residual porosity Si, and when ruined so that surface surface smoothness is nonpermissible, after it performs surface flattening, it can be again used for it as 1st Si single crystal substrate 31.

[0074] As shown in [example 4 of embodiment] drawing 4 (a), 1st Si single crystal substrate 41 is prepared first, the surface layer is carried out porosity-ized 42, and the nonvesicular single crystal compound semiconductor layer 43 is formed on porosity Si 42 (drawing 4 (b)).

[0075] Next, as shown in drawing 4 (c), after sticking the light transmission nature support substrate 44 and the single crystal compound semiconductor layer 43 which are represented by a quartz and glass at a room temperature through an insulating layer 45, it sticks with anode plate junction, pressurization, heat treatments, or such combination. This combines firmly the light transmission nature support substrate 44 and the single crystal layer 43 through an insulating layer 45. Or it forms an insulating layer 45 at least in one side on a single crystal compound semiconductor layer and the light transmission nature support substrate 44, it is stuck by the three-sheet pile on both sides of insulating sheet metal.

[0076] Next, a substrate is divided in the porosity Si layer 43 (drawing 4 (d)). A light transmission nature support substrate side serves as structure like the 45/light transmission nature support substrate 44 of 43/insulating layers of porosity Si42/single crystal compound semiconductor layers.

[0077] Furthermore, porosity Si 42 is removed alternatively. Chemical etching of the porosity Si 42 is carried out using an etching reagent with the quick etch rate of Si to a compound semiconductor, and on insulating substrate 45 +44, the thin-film-ized single crystal compound semiconductor layer 43 is made to remain, and it forms.

[0078] Or porosity Si 42 is removed by selection polish by using the single crystal compound semiconductor layer 43 as a polish stopper.

[0079] The semi-conductor substrate obtained by this invention is shown in drawing 4 (e). On light transmission nature insulation substrate 45 +44, evenly, lamination of the single crystal compound semiconductor layer 43 is carried out to homogeneity, and it is formed throughout a wafer at a large area. In this way, the obtained semi-conductor substrate can be suitably used, even if it sees from the point of electronic device production by which insulating separation was carried out.

[0080] There may not be the insulating mediation layer 45.

[0081] 1st Si single crystal substrate 41 removes the residual porosity Si, and when ruined so that surface surface smoothness is nonpermissible, after it performs surface flattening, it can be again used for it as 1st Si single crystal substrate 41.

[0082] it is shown in [example 5 of embodiment] drawing 5 (a) -- as -- first -- 1st Si single crystal substrate 51 -- preparing -- the surface layer of the both sides -- the porosity-izing 52 -- 53 are taken and the nonvesicular single crystal half conductor layers 54 and 55 are formed on the double-sided porosity Si 52 and 53 (drawing 5 (b)).

[0083] Next, as shown in drawing 5 (c), after sticking two support substrates 56 and 57 and the single crystal half conductor layers 54 and 55 at a room temperature through insulating layers 58 and 59, respectively, it sticks with anode plate junction, pressurization, heat treatments, or such combination. This combines firmly the support substrates 56 and 57 and the single crystal layers 54 and 55 through insulating layers 58 and 59. Or it forms insulating layers 58 and 59 at least in one side on the support substrate 56 and 67 on the single crystal half conductor layer 54 and 55, they are stuck by the five-sheet pile on both sides of insulating sheet metal.

[0084] Next, a substrate is trichotomized in both the porosity Si layers 52 and 53 (drawing 5 (d)). Two support substrates serve as structure like porosity Si / single crystal half conductor layer / insulating layer / support substrate (52/54/58/56, and 53/55/59/57).

[0085] Furthermore, both the porosity 52 and Si 53 is removed alternatively. Chemical etching of the porosity 52 and Si 53 is carried out alternatively, and on the support substrates 58/56, and 59/57, the thin-film-ized single crystal half conductor layers 54 and 55 are made to remain, and it forms.

[0086] Or porosity 52 and Si 53 is removed by selection and polish by using the single crystal half conductor layers 54 and 55 as a polish stopper.

[0087] The semi-conductor substrate obtained by this invention is shown in drawing 5 (e). On a support substrate, evenly, lamination of the single crystal compound semiconductor layer is carried out to homogeneity, and it is formed throughout a wafer at two-body coincidence at a large area. In this way, the obtained semi-conductor substrate can be suitably used, even if it sees from the point of electronic device production by which insulating separation was carried out.

[0088] There may not be the insulating mediation layers 58 and 59.

[0089] The support substrates 56 and 57 may not be the same.

[0090] 1st Si single crystal substrate 51 removes the residual porosity Si, and when ruined so that surface smoothness is nonpermissible, after it performs surface flattening, it can be again used for it as 1st Si single crystal 51.

[0091]

[Example]

(Example 1) Anodization was performed for the 1st single crystal (100) Si substrate of the diameter of 6 inch of the P type with the thickness of 625 micrometers of specific resistance 0.01 ohm-cm into HF solution.

[0092] The anodization conditions were as follows.

[0093] Current density: 5 (mA-cm⁻²)

anodization solution: -- HF:H₂O:C₂H₅OH=1:1:1 hour: -- 12 (minute)

Thickness of Porosity Si: 10 (micrometer)

Porosity:15(%)

This substrate was oxidized at 400 degrees C among the oxygen ambient atmosphere for 1 hour. The wall of the hole of Porosity Si was covered with this oxidation by the thermal oxidation film. Porosity Si top -- CVD (Chemical Vapor Deposition) -- 1 micrometer grew the single crystal Si epitaxially by law. The growth conditions are as follows.

[0094] source gas: -- SiH₂Cl₂ / H₂ quantity-of-gas-flow: -- 0.5/180 l/min gas pressure: -- 80Torr temperature: -- 950-degree-C growth rate: -- it formed 100nm SiO₂ two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.3 micrometer/min pan.

[0095] This SiO₂ 500nm SiO₂ prepared apart from the layer front face Superposition and after making it contact, heat treatment of 900 degrees C - 2 hours was carried out for the front face of Si substrate in which the layer was formed, and lamination was performed.

[0096] When sufficient hauling force for homogeneity was perpendicularly applied to the field of the stuck wafer, the porosity Si layer broke, the wafer was halved and Porosity Si expressed it. Adhesives were used, the plate was specifically pasted up on both sides of the stuck wafer, and after arranging this plate on the fixture made to move in the direction which pulls apart this plate of each other, it was pulled apart in two.

[0097] Then, selective etching was carried out, agitating a porosity Si layer 49% with the mixed liquor (1:5) of fluoric acid and 30% hydrogen peroxide solution. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the porosity Si was carried out, and the single crystal Si was removed completely.

[0098] The etch rate to this etching reagent of a nonvesicular Si single crystal is very low, the selection ratio with the etch rate of a porous layer amounts to the fifth power or more of 10, and the amount of etching in a nonvesicular layer (about dozens of Å) is thickness reduction which can be disregarded practically.

[0099] That is, the single crystal Si layer which had the thickness of 1 micrometer on Si oxide film has been formed. It was changeless in a single crystal Si layer in any way also by the selective etching of Porosity Si.

[0100] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.

[0101] In this way, the SOI substrate which has a quality semi-conductor layer was obtained.

Furthermore, after the same etching removed the porous layer which remains in Si substrate of another side separated bordering on the porosity Si layer, polishing of the front face was carried out. In this way, the SOI substrate plurality which has a quality semi-conductor layer was obtained by repeating an above-mentioned process using obtained Si substrate.

[0102] (Example 2) Anodization was performed for the 1st single crystal (100) Si substrate of the diameter of 4 inch of the P type with the thickness of 525 micrometers of specific resistance 0.01 ohm-cm into HF solution.

[0103] The anodization conditions were as follows.

[0104] Current density: 7 (mA-cm⁻²)

anodization solution: -- HF:H₂O:C₂H₅OH=1:1:1 hour: -- 12 (minute)

Thickness of Porosity Si: 10 (micrometer)

Porosity:15(%)

This substrate was oxidized at 400 degrees C among the oxygen ambient atmosphere for 2 hours. The wall of the hole of Porosity Si was covered with this oxidation by the thermal oxidation film. Porosity Si top -- MBE (Molecular Beam Epitaxy) -- 0.5 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.

[0105] temperature: -- 700-degree-C pressure: -- 1×10^{-9} Torr growth rate: -- 0.1 nm/sec temperature: -- 950-degree-C growth rate: -- it formed 100nm SiO₂ two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.3 micrometer/min pan.

[0106] This SiO₂ Superposition and after making it contact, heat treatment of 400 degrees C - 2 hours was carried out for the layer front face and the front face of the fused-quartz substrate prepared independently, and lamination was performed.

[0107] When sufficient pressure for homogeneity was perpendicularly applied to the field of the stuck wafer, the porosity Si layer broke, the wafer was halved and Porosity Si expressed it. Adhesives were used, the plate was specifically pasted up on both sides of the stuck wafer, and after arranging this plate on the fixture which stated this plate in the example 1, Si layer was destroyed by applying a pressure to this plate.

[0108] Then, selective etching is carried out, agitating a porosity Si layer with the mixed liquor (1:5) of buffered fluoric acid and 30% hydrogen peroxide solution. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the porosity Si was carried out, and the single crystal Si was removed completely.

[0109] The etch rate to this etching reagent of a nonvesicular Si single crystal is very low, the selection ratio with the etch rate of a porous layer amounts to the fifth power or more of 10, and the amount of etching in a nonvesicular layer (about dozens of A) is thickness reduction which can be disregarded practically.

[0110] That is, the single crystal Si layer which had the thickness of 0.5 micrometers on the fused-quartz substrate has been formed. It was changeless in a single crystal Si layer in any way also by the selective etching of Porosity Si.

[0111] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.

[0112] The SOI substrate plurality which has a quality semi-conductor layer by repeating an above-mentioned process like an example 1 was obtained.

[0113] (Example 3) Anodization was performed for the 1st single crystal (100) Si substrate of the diameter of 6 inch of the P type with the thickness of 625 micrometers of specific resistance 0.01 ohm-cm, or N type into HF solution.

[0114] The anodization conditions were as follows.

[0115] Current density: 7 (mA-cm⁻²)

anodization solution: -- HF:H₂O:C₂H₅OH=1:1:1 hour: -- 12 (minute)

Thickness of Porosity Si: 10 (micrometer)

Porosity:15(%)

This substrate was oxidized at 400 degrees C among the oxygen ambient atmosphere for 1 hour. The wall of the hole of Porosity Si was covered with this oxidation by the thermal oxidation film. Porosity Si top -- MOCVD (MetalOrganic Chemical Vapor Deposition) -- 1 micrometer grew the single crystal GaAs epitaxially by law. The growth conditions are as follows.

[0116] source gas: -- TMG/AsH₃ / H₂ gas-pressure: -- 80Torr temperature: -- superposition and after making it contact, heat treatment of 900 degrees C - 1 hour was carried out for 700-degree-C this GaAs layer front face and the front face of 2nd Si substrate prepared independently, and lamination was performed. Both substrates were firmly stuck by this heat treatment.

[0117] When the pressure was applied to the stuck wafer like the example 2, the porosity Si layer broke, the wafer was halved and Porosity Si expressed it.

[0118] Then, after removing the oxide film of a wall for a porosity Si layer by fluoric acid, Porosity Si was etched by 110 degrees C (ratio of 17ml : 3g : 8ml) of ethylenediamine + pyrocatechol + water. The single crystal GaAs remained without being etched, as an ingredient of a dirty stop, selective etching of the porosity Si was carried out, and the single crystal GaAs was removed completely.

[0119] The etch rate to this etching reagent of a single crystal GaAs is very low, and is thickness reduction which can be disregarded practically.

[0120] That is, the single crystal GaAs layer which had the thickness of 1 micrometer on Si substrate has been formed. It was changeless in a single crystal GaAs layer in any way also by the selective etching of Porosity Si.

[0121] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into a GaAs layer, but it was checked that good crystallinity is maintained.

[0122] Like the example 2, the above-mentioned process was repeated and two or more semi-conductor substrates which allotted the quality GaAs layer were obtained.

[0123] By using Si substrate with an oxide film as a support substrate, GaAs on an insulator layer was producible similarly.

[0124] (Example 4) Anodization was performed for the 1st single crystal (100) Si substrate of the diameter of 5 inch of the P type with the thickness of 625 micrometers of specific resistance 0.01 ohm-cm, or N type into HF solution.

[0125] The anodization conditions were as follows.

[0126] Current density: 10 (mA-cm⁻²)

anodization solution: -- HF:H₂O:C₂H₅OH=1:1:1 hour: -- 24 (minute)

Thickness of Porosity Si: 20 (micrometer)

Porosity: 17(%)

This substrate was oxidized at 400 degrees C among the oxygen ambient atmosphere for 2 hours. The wall of the hole of Porosity Si was covered with this oxidation by the thermal oxidation film. Porosity Si top -- MBE (Molecular Beam Epitaxy) -- 0.5 micrometers grew the single crystal AlGaAs epitaxially by law.

[0127] Superposition and after making it contact, heat treatment of 500 degrees C - 2 hours was carried out for this AlGaAs layer front face and the front face of the low-melting-glass substrate prepared independently, and lamination was performed. Both substrates were firmly stuck by this heat treatment.

[0128] When the pressure was applied like the stuck wafer example 2, the porosity Si layer broke, the wafer was halved and Porosity Si expressed it.

[0129] Then, Porosity Si was etched with the fluoric acid solution. The single crystal AlGaAs remained without being etched, as an ingredient of a dirty stop, selective etching of the porosity Si was carried out, and the single crystal AlGaAs was removed completely.

[0130] The etch rate to this etching reagent of a single crystal AlGaAs is very low, and is thickness reduction which can be disregarded practically.

[0131] That is, the single crystal AlGaAs layer which had the thickness of 0.5 micrometers on the glass substrate has been formed. It was changeless in a single crystal AlGaAs layer in any way also by the selective etching of Porosity Si.

[0132] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into an AlGaAs layer, but it was checked that good crystallinity is maintained. Two or more substrates which have a quality semi-conductor layer by repeating an above-mentioned process like an example 2 were obtained.

[0133] (Example 5) Anodization was performed for the 1st single crystal (100) Si substrate of the diameter of 6 inch of double-sided polish of the P type with the thickness of 625 micrometers of specific resistance 0.01 ohm-cm, or N type to both sides into HF solution.

[0134] The anodization conditions were as follows.

[0135] Current density: 5 (mA-cm⁻²)

anodization solution: -- HF:H₂O:C₂H₅OH=1:1:1 hour: -- 12x2 (minute)

Thickness of Porosity Si: Each 10 (micrometer)

Porosity:15(%)

This substrate was oxidized at 400 degrees C among the oxygen ambient atmosphere for 1 hour. The wall of the hole of Porosity Si was covered with this oxidation by the thermal oxidation film. the porosity Si top formed in both sides -- CVD (Chemical Vapor Deposition) -- 1 micrometer grew the single crystal Si epitaxially by law, respectively. The growth conditions are as follows.

[0136] source gas: -- SiH₂ Cl₂ / H₂ quantity-of-gas-flow: -- 0.5/180 l/min gas pressure: -- 80Torr temperature: -- 950-degree-C growth rate: -- it formed 100nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.3 micrometer/min pan.

[0137] This SiO₂ 500nm SiO₂ prepared apart from the layer front face Superposition and after making it contact, heat treatment of 600 degrees C - 2 hours was carried out for the front face of two Si substrates in which the layer was formed, respectively, and lamination was performed.

[0138] When perpendicularly sufficient hauling force was applied to the field of the wafer stuck using the technique of an example 1, the porosity Si layer destroyed two-layer, the wafer was trichotomized and Porosity Si expressed it.

[0139] Then, selective etching is carried out, agitating a porosity Si layer 49% with the mixed liquor (1:5) of fluoric acid and 30% hydrogen peroxide solution. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the porosity Si was carried out, and the single crystal Si was removed completely.

[0140] the etch rate to this etching reagent of a nonvesicular Si single crystal -- very -- low -- the selection ratio with the etch rate of a porous layer -- the fifth power or more of 10 -- reaching -- a ratio -- the amount of etching in a porous layer (about dozens of A) is thickness reduction which can be disregarded practically.

[0141] That is, the single crystal Si layer which had the thickness of 1 micrometer on Si oxide film has formed in two-sheet coincidence. It was changeless in a single crystal Si layer in any way also by the selective etching of Porosity Si.

[0142] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained. The above-mentioned process as well as an example 1 was repeated, and the substrate plurality which has a quality semi-conductor layer was obtained.

[0143] (Example 6) Anodization was performed for the 1st single crystal (100) Si substrate of the diameter of 5 inch of the P type with the thickness of 625 micrometers of specific resistance 0.01 ohm-cm, or N type into HF solution.

[0144] The anodization conditions were as follows.

[0145] Current density: 7 (mA-cm⁻²)

anodization solution: -- HF:H₂ O:C₂ H₅ OH=1:1:1 hour: -- 4 (minute)

Thickness of Porosity Si: 3 (micrometer)

Porosity:15(%)

Furthermore, current density: 30 (mA-cm⁻²)

anodization solution: -- HF:H₂ O:C₂ H₅ OH=1:3:2 hour: -- 3 (minute)

Thickness of Porosity Si: 10 (micrometer)

Porosity:45(%)

This substrate was oxidized at 400 degrees C among the oxygen ambient atmosphere for 1 hour. The wall of the hole of Porosity Si was covered with this oxidation by the thermal oxidation film. 0.3 micrometers grew the single crystal Si epitaxially with the CVD method on Porosity Si. The growth conditions are as follows.

[0146] source gas: -- SiH₄ carrier gas: -- H₂ temperature: -- 850-degree-C pressure: -- 1x10⁻²Torr growth rate: -- it formed 100nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation further 3.3 nm/sec.

[0147] This SiO₂ 500nm SiO₂ prepared apart from the layer front face Superposition and after making it contact, heat treatment of 700 degrees C - 2 hours was carried out for the front face of Si substrate in

which the layer was formed, and lamination was performed.

[0148] The porosity Si layer broke in the place which applied perpendicularly sufficient hauling force to the field of the stuck wafer using the technique of an example 1, the wafer was halved and Porosity Si expressed it.

[0149] Then, selective etching of the porosity Si layer is carried out with the etching reagent of HF/HNO₃ / CH₃ COOH system. Porosity Si was etched and was removed completely.

[0150] The etch rate to this etching reagent of a nonvesicular Si single crystal is very low, and the amount of etching in a nonvesicular layer is thickness reduction which can be disregarded practically.

[0151] That is, the single crystal Si layer which had the thickness of 1 micrometer on Si oxide film has been formed. It was changeless in a single crystal Si layer in any way also by the selective etching of Porosity Si.

[0152] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained. The above-mentioned process as well as an example 1 was repeated, and the substrate plurality which has a quality semi-conductor layer was obtained.

[0153] (Example 7) Anodization was performed for the 1st single crystal (100) Si substrate of the diameter of 6 inch of the P type with the thickness of 625 micrometers of specific resistance 0.01 ohm-cm, or N type into HF solution.

[0154] The anodization conditions were as follows.

[0155] Current density: 5 (mA-cm⁻²)

anodization solution: -- HF:H₂O:C₂H₅OH=1:1:1 hour: -- 12 (minute)

Thickness of Porosity Si: 10 (micrometer)

Porosity:15(%)

This substrate was oxidized at 400 degrees C among the oxygen ambient atmosphere for 1 hour. The wall of the hole of Porosity Si was covered with this oxidation by the thermal oxidation film. Porosity Si top -- CVD (Chemical Vapor Deposition) -- 1 micrometer grew the single crystal Si epitaxially by law. The growth conditions are as follows.

[0156] source gas: -- SiH₂Cl₂ / H₂ quantity-of-gas-flow: -- 0.5/180 l/min gas pressure: -- 80Torr temperature: -- 950-degree-C growth rate: -- it formed 100nm SiO₂ two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.3 micrometer/min pan.

[0157] This SiO₂ 500nm SiO₂ prepared apart from the layer front face Superposition and after making it contact, heat treatment of 900 degrees C - 2 hours was carried out for the front face of Si substrate in which the layer was formed, and lamination was performed.

[0158] When perpendicularly sufficient hauling force was applied to the field of the stuck wafer using the technique of an example 1, the porosity Si layer broke, the wafer was halved and Porosity Si expressed it.

[0159] Then, selection polish of the porosity Si layer was carried out, having used the single crystal Si as the stopper. Porosity Si selection polish was carried out and it was removed completely.

[0160] That is, the single crystal Si layer which had the thickness of 1 micrometer on Si oxide film has been formed. It was changeless in a single crystal Si layer in any way also by the selective etching of Porosity Si.

[0161] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained. The above-mentioned process as well as an example 1 was repeated, and the substrate plurality which has a quality semi-conductor layer was obtained.

[0162] (Example 8) Anodization was performed for the 1st single crystal (100) Si substrate of the diameter of 6 inch of the P type with the thickness of 625 micrometers of specific resistance 0.01 ohm-cm, or N type into HF solution.

[0163] The anodization conditions were as follows.

[0164] Current density: 5 (mA-cm⁻²)

anodization solution: -- HF:H₂O:C₂H₅OH=1:1:1 hour: -- 12 (minute)

Thickness of Porosity Si: 10 (micrometer)

Porosity:15(%)

This substrate was oxidized at 400 degrees C among the oxygen ambient atmosphere for 1 hour. The wall of the hole of Porosity Si was covered with this oxidation by the thermal oxidation film. Porosity Si top -- CVD (Chemical Vapor Deposition) -- 1 micrometer grew the single crystal Si epitaxially by law. The growth conditions are as follows.

[0165] source gas: -- SiH₂ Cl₂ / H₂ quantity-of-gas-flow: -- 0.5/180 l/min gas pressure: -- 80Torr temperature: -- 950-degree-C growth rate: -- it formed 100nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.3 micrometer/min pan.

[0166] This SiO₂ 500nm SiO₂ prepared apart from the layer front face Superposition and after making it contact, heat treatment of 900 degrees C - 2 hours was carried out for the front face of Si substrate in which the layer was formed, and lamination was performed. Subsequently, when the stuck substrate was put in into the layer which arranged the ultrasonic vibrator and ultrasonic energy was impressed, the porosity Si layer broke, the wafer was halved and Porosity Si expressed it.

[0167] Then, selective etching is carried out, agitating a porosity Si layer 49% with the mixed liquor (1:5) of fluoric acid and 30% hydrogen peroxide solution. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the porosity Si was carried out, and the single crystal Si was removed completely.

[0168] The etch rate to this etching reagent of a nonvesicular Si single crystal is very low, the selection ratio with the etch rate of a porous layer amounts to the fifth power or more of 10, and the amount of etching in a nonvesicular layer (about dozens of A) is thickness reduction which can be disregarded practically.

[0169] That is, the single crystal Si layer which had the thickness of 1 micrometer on Si oxide film has been formed. It was changeless in a single crystal Si layer in any way also by the selective etching of Porosity Si.

[0170] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.

[0171] 1st Si single crystal substrate removed the residual porosity Si, and used it as 1st Si single crystal substrate again.

[0172] (Example 9) Anodization was performed for the 1st single crystal (100) Si substrate of the diameter of 4 inch of the P type with the thickness of 525 micrometers of specific resistance 0.01 ohm-cm, or N type into HF solution.

[0173] The anodization conditions were as follows.

[0174] Current density: 7 (mA-cm⁻²)

anodization solution: -- HF:H₂O:C₂H₅OH=1:1:1 hour: -- 12 (minute)

Thickness of Porosity Si: 10 (micrometer)

Porosity:15(%)

This substrate was oxidized at 400 degrees C among the oxygen ambient atmosphere for 2 hours. The wall of the hole of Porosity Si was covered with this oxidation by the thermal oxidation film. Porosity Si top -- MBE (Molecular Beam Epitaxy) -- 0.5 micrometers grew the single crystal Si epitaxially by law. The growth conditions are as follows.

[0175] temperature: -- 700-degree-C pressure: -- 1x10⁻⁹Torr growth rate: -- 0.1 nm/sec temperature: -- 950-degree-C growth rate: -- it formed 100nm SiO two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.3 micrometer/min pan.

[0176] This SiO₂ Superposition and after making it contact, heat treatment of 400 degrees C - 2 hours was carried out for the layer front face and the front face of the fused-quartz substrate prepared independently, and lamination was performed.

[0177] The wafer end face was made to express a porous layer, when Porosity Si was etched to some extent and the sharp plate was inserted there like the cutting edge of a razor, the porosity Si layer broke, the wafer was halved and Porosity Si expressed it.

[0178] Then, selective etching is carried out, agitating a porosity Si layer with the mixed liquor (1:5) of

buffered fluoric acid and 30% hydrogen peroxide solution. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the porosity Si was carried out, and the single crystal Si was removed completely.

[0179] The etch rate to this etching reagent of a nonvesicular Si single crystal is very low, the selection ratio with the etch rate of a porous layer amounts to the fifth power or more of 10, and the amount of etching in a nonvesicular layer (about dozens of Å) is thickness reduction which can be disregarded practically.

[0180] That is, the single crystal Si layer which had the thickness of 0.5 micrometers on the fused-quartz substrate has been formed. It was changeless in a single crystal Si layer in any way also by the selective etching of Porosity Si.

[0181] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.

[0182] The same result was obtained even if it did not form an oxide film in the epitaxial Si layer front face.

[0183] 1st Si single crystal substrate removed the residual porosity Si, and after performing surface polish and making it the shape of a mirror plane, it used it as 1st Si single crystal substrate again.

[0184] (Example 10) Anodization was performed for the 1st single crystal (100) Si substrate of the diameter of 6 inch of double-sided polish of the P type with the thickness of 625 micrometers of specific resistance 0.01 ohm-cm, or N type to both sides into HF solution.

[0185] The anodization conditions were as follows.

[0186] Current density: 5 (mA-cm⁻²)

anodization solution: -- HF:H₂O:C₂H₅OH=1:1:1 hour: -- 12x2 (minute)

Thickness of Porosity Si: Each 10 (micrometer)

Porosity:15(%)

This substrate was oxidized at 400 degrees C among the oxygen ambient atmosphere for 1 hour. The wall of the hole of Porosity Si was covered with this oxidation by the thermal oxidation film. the porosity Si top formed in both sides -- CVD (Chemical Vapor Deposition) -- 1 micrometer grew the single crystal Si epitaxially by law. The growth conditions are as follows.

[0187] source gas: -- SiH₂Cl₂ / H₂ quantity-of-gas-flow: -- 0.5/180 l/min gas pressure: -- 80Torr temperature: -- 950-degree-C growth rate: -- it formed 100nm SiO₂ two-layer in this epitaxial Si layer front face by thermal oxidation at the 0.3 micrometer/min pan.

[0188] This SiO₂ 500nm SiO₂ prepared apart from the layer front face Superposition and after making it contact, heat treatment of 600 degrees C - 2 hours was carried out for the front face of two Si substrates in which the layer was formed, respectively, and lamination was performed.

[0189] After making the wafer end face express a porous layer and infiltrating liquids, such as water, into a porous layer Si, when the whole lamination wafer was heated or cooled, the porosity Si layer broke by expansion of a liquid etc., the wafer was halved and Porosity Si expressed it.

[0190] Then, selective etching is carried out, agitating a porosity Si layer 49% with the mixed liquor (1:5) of fluoric acid and 30% hydrogen peroxide solution. The single crystal Si remained without being etched, as an ingredient of a dirty stop, selective etching of the porosity Si was carried out, and the single crystal Si was removed completely.

[0191] The etch rate to this etching reagent of a nonvesicular Si single crystal is very low, the selection ratio with the etch rate of a porous layer amounts to the fifth power or more of 10, and the amount of etching in a nonvesicular layer (about dozens of Å) is thickness reduction which can be disregarded practically.

[0192] That is, the single crystal Si layer which had the thickness of 1 micrometer on Si oxide film has formed in two-sheet coincidence. It was changeless in a single crystal Si layer in any way also by the selective etching of Porosity Si.

[0193] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.

[0194] The same result was obtained even if it did not form an oxide film in the epitaxial Si layer front

face.

[0195] 1st Si single crystal substrate removed the residual porosity Si, and after it carried out hydrogen processing and carried out flattening of the front face, it used it as 1st Si single crystal substrate again.

[0196] (Example 11) Anodization was performed for the 1st single crystal (100) Si substrate of the diameter of 5 inch of the P type with the thickness of 625 micrometers of specific resistance 0.01 ohm-cm, or N type into HF solution.

[0197] The anodization conditions were as follows.

[0198] Current density: 7 (mA-cm⁻²)

anodization solution: -- HF:H₂O:C₂H₅OH=1:1:1 hour: -- 4 (minute)

Thickness of Porosity Si: 3 (micrometer)

Porosity:15(%)

Furthermore, current density: 30 (mA-cm⁻²)

anodization solution: -- HF:H₂O:C₂H₅OH=1:3:2 hour: -- 3 (minute)

Thickness of Porosity Si: 10 (micrometer)

Porosity:45(%)

This substrate was oxidized at 400 degrees C among the oxygen ambient atmosphere for 1 hour. The wall of the hole of Porosity Si was covered with this oxidation by the thermal oxidation film. 0.3 micrometers grew the single crystal Si epitaxially with the CVD method on Porosity Si. The growth conditions are as follows.

[0199] source gas: -- SiH₄ carrier gas: -- H₂ temperature: -- 850-degree-C pressure: -- 1x10⁻²Torr

growth rate: -- it formed 100nm SiO₂ two-layer in this epitaxial Si layer front face by thermal oxidation further 3.3 nm/sec.

[0200] This SiO₂ 500nm SiO₂ prepared apart from the layer front face Superposition and after making it contact, heat treatment of 700 degrees C - 2 hours was carried out for the front face of Si substrate in which the layer was formed, and lamination was performed.

[0201] When the force was horizontally applied to the 2nd (or the 1st) substrate to the 1st (or the 2nd) substrate, a porosity Si layer could not finish bearing shearing stress, and it destroyed, and the wafer was halved and Porosity Si expressed it.

[0202] Then, selective etching of the porosity Si layer is carried out with the etching reagent of HF/HNO₃ / CH₃COOH system. Selective etching of the porosity Si was carried out, and it was removed completely.

[0203] The etch rate to this etching reagent of a nonvesicular Si single crystal is very low, and the amount of etching in a nonvesicular layer is thickness reduction which can be disregarded practically.

[0204] That is, the single crystal Si layer which had the thickness of 1 micrometer on Si oxide film has been formed. It was changeless in a single crystal Si layer in any way also by the selective etching of Porosity Si.

[0205] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.

[0206] The same result was obtained even if it did not form an oxide film in the epitaxial Si layer front face.

[0207] 1st Si single crystal substrate removed the residual porosity Si, and used it as 1st Si single crystal substrate again.

[0208] (Example 12) Anodization was performed for the 1st single crystal (100) Si substrate of the diameter of 5 inch of the P type with the thickness of 625 micrometers of specific resistance 0.01 ohm-cm, or N type into HF solution.

[0209] The anodization conditions were as follows.

[0210] Current density: 7 (mA-cm⁻²)

anodization solution: -- HF:H₂O:C₂H₅OH=1:1:1 hour: -- 4 (minute)

Thickness of Porosity Si: 3 (micrometer)

Porosity:15(%)

Furthermore, current density: 30 (mA-cm⁻²)

anodization solution: -- HF:H₂O:C₂H₅OH=1:3:2 hour: -- 3 (minute)

Thickness of Porosity Si: 10 (micrometer)

Porosity:45(%)

This substrate was oxidized at 400 degrees C among the oxygen ambient atmosphere for 1 hour. The wall of the hole of Porosity Si was covered with this oxidation by the thermal oxidation film. 0.3 micrometers grew the single crystal Si epitaxially with the CVD method on Porosity Si. The growth conditions are as follows.

[0211] source gas: -- SiH₄ carrier gas: -- H₂ temperature: -- 850-degree-C pressure: -- 1x10⁻²Torr growth rate: -- it formed 100nm SiO₂ two-layer in this epitaxial Si layer front face by thermal oxidation further 3.3 nm/sec.

[0212] This SiO₂ 500nm SiO₂ prepared apart from the layer front face Superposition and after making it contact, heat treatment of 700 degrees C - 2 hours was carried out for the front face of Si substrate in which the layer was formed, and lamination was performed.

[0213] The wafer end face was made to express a porous layer, and the wafer was halved when the porosity Si layer was etched from the end face with the selection etching reagent of Porosity Si.

[0214] Then, selective etching of the porosity Si layer is carried out with the etching reagent of HF/HNO₃ / CH₃ COOH system. Selective etching of the porosity Si was carried out, and it was removed completely.

[0215] The etch rate to this etching reagent of a nonvesicular Si single crystal is very low, and the amount of etching in a nonvesicular layer is thickness reduction which can be disregarded practically.

[0216] That is, the single crystal Si layer which had the thickness of 1 micrometer on Si oxide film has been formed. It was changeless in a single crystal Si layer in any way also by the selective etching of Porosity Si.

[0217] As a result of the cross-section observation by the transmission electron microscope, a new crystal defect was not introduced into Si layer, but it was checked that good crystallinity is maintained.

[0218] The same result was obtained even if it did not form an oxide film in the epitaxial Si layer front face.

[0219] 1st Si single crystal substrate removed the residual porosity Si, and used it as 1st Si single crystal substrate again.

[0220]

[Effect of the Invention] As explained above, according to this invention, it sticks, the constituted base is separated by the porous layer, and the semi-conductor base with which the quality nonvesicular single crystal half conductor layer was allotted can be formed by removing the porous layer on the 2nd base to which the nonvesicular single crystal half conductor layer was allotted.

[0221] In addition, it sticks and the constituted base is separated by the porous layer, and since the 1st base from which the porous layer was removed by removing the porous layer which constitutes the 1st base is reusable to semi-conductor base production, improvement in the productivity of a semi-conductor base and low cost-ization can be attained further.

[0222] Moreover, according to this invention, the production approach of the semi-conductor substrate which stood high in the field of productivity, homogeneity, a controllability, and cost on substrates including a transparency substrate (light transmission nature substrate) when crystallinity obtained a single crystal layer or compound semiconductor single crystal layers, such as Si which was excellent just like the single crystal wafer, can be proposed.

[0223] Moreover, according to this invention, also in case the large-scale integrated circuit of SOI structure is produced, the production approach of expensive SOS and the alternative ***** substrate of SIMOX can be proposed.

[0224] Moreover, a base is separable into two or more through a porous layer, and after one base after separation removes residual porosity, it is usable as a semi-conductor substrate, and after removing residual porosity, it is applicable [the base of another side] to production of a semi-conductor substrate according to this invention, again.

[0225] Moreover, a porous layer and a nonvesicular single crystal layer are formed in both sides of a

base, and after sticking another base of two sheets so that this single crystal layer may be pinched, two semi-conductor substrates are producible to coincidence according to this invention, by separating a base by said porous layer.

[0226] namely, -- according to this invention -- economical efficiency -- excelling -- a large area -- crossing -- homogeneity -- it can leave the semi-conductor layer or compound semiconductor barrier layer formed in the front face using the flat single crystal substrate which has the extremely excellent crystallinity, this from the one side to barrier layer can be removed, and the production approach of a semi-conductor substrate of obtaining few remarkable single crystal layers or compound semiconductor crystal layer of a defect to an insulating lifter can be offered.

[0227] Moreover, the production approach of the semi-conductor substrate which stood high in the field of productivity, homogeneity, a controllability, and cost on the transparence substrate (light transmission nature substrate) when crystallinity obtained Si which was excellent just like the single crystal wafer, or a compound semiconductor single crystal layer can be acquired.

[0228] Moreover, also in case the large-scale integrated circuit of SOI structure is produced, the production approach of expensive SOS and the alternative ***** substrate of SIMOX can be acquired.

[Translation done.]

* NOTICES *

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is a typical sectional view for explaining one example of the approach of this invention.

[Drawing 2] It is a typical sectional view for explaining one example of the approach of this invention.

[Drawing 3] It is a typical sectional view for explaining one example of the approach of this invention.

[Drawing 4] It is a typical sectional view for explaining one example of the approach of this invention.

[Drawing 5] It is a typical sectional view for explaining one example of the approach of this invention.

[Description of Notations]

11 Si Single Crystal Substrate

12 Porosity Si Layer

13 Nonvesicular Single Crystal Si Layer

14 Si Support Substrate

15 Insulating Layer

[Translation done.]

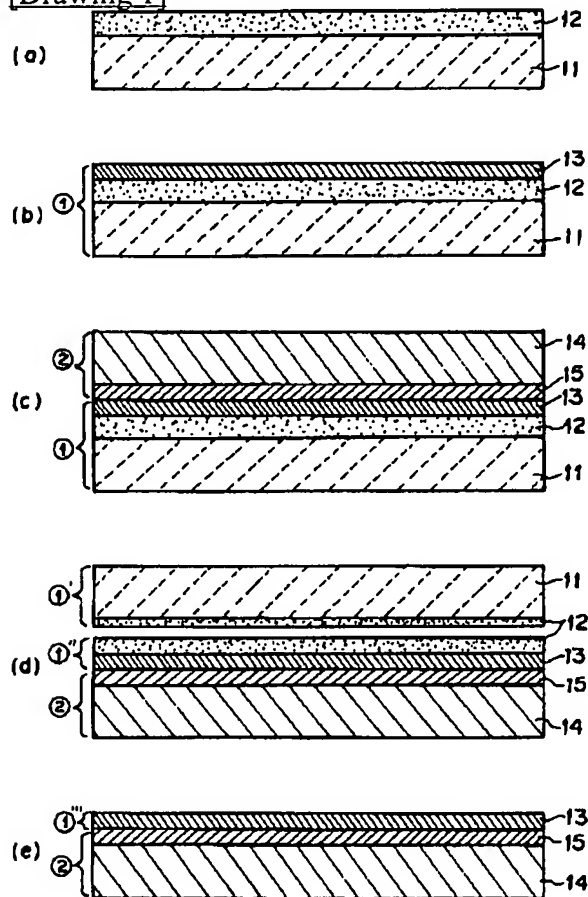
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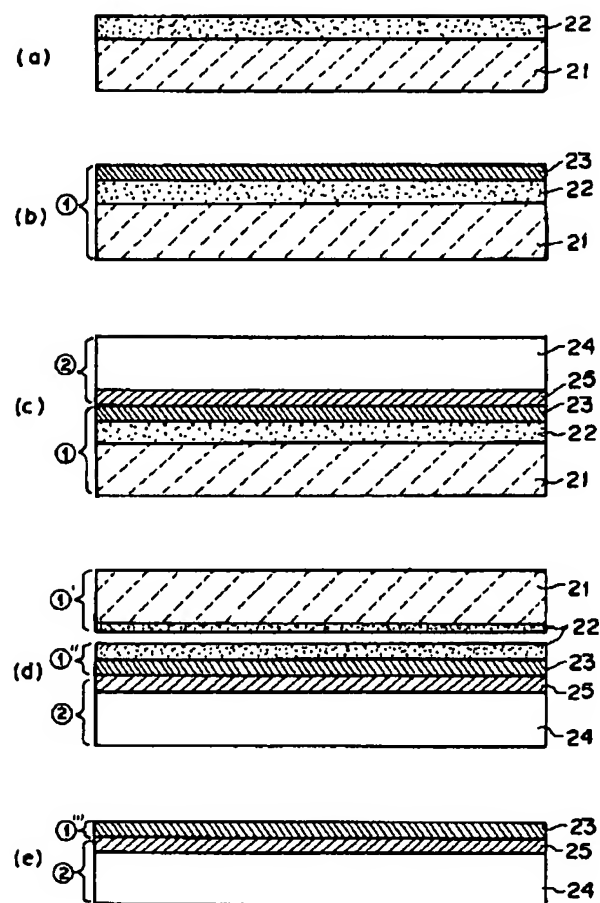
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DRAWINGS

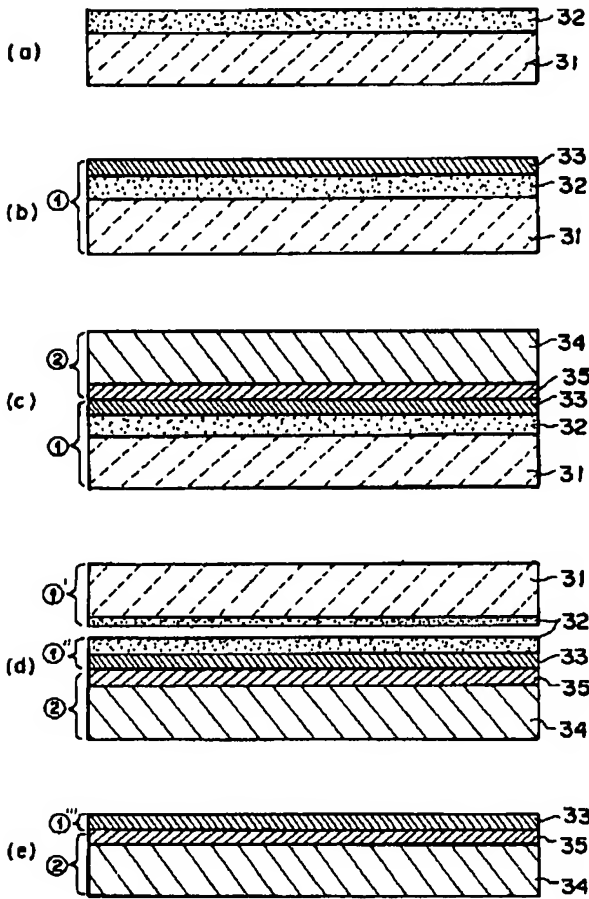
[Drawing 1]



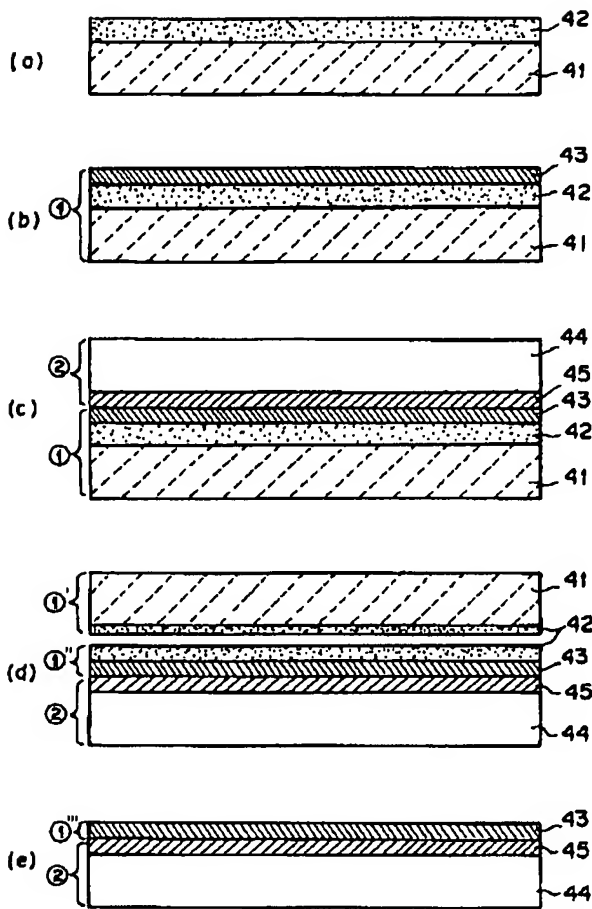
[Drawing 2]



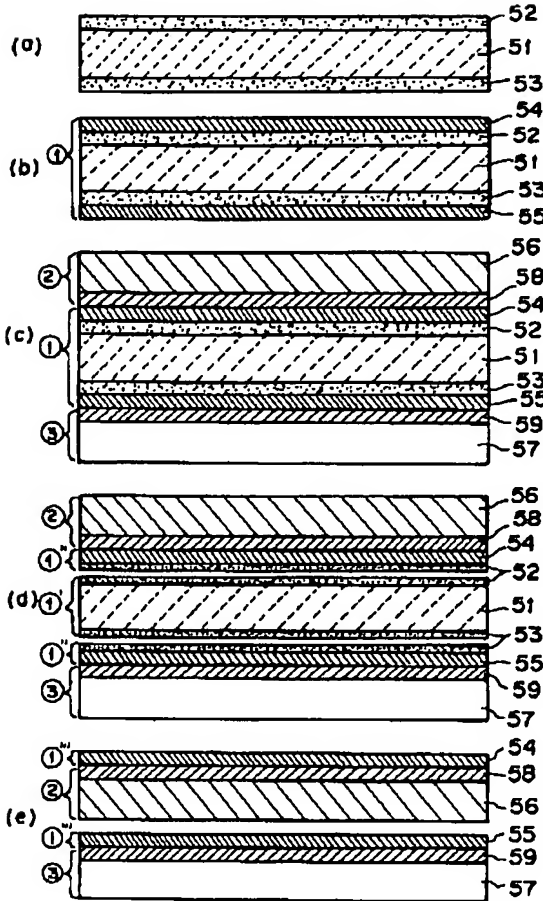
[Drawing 3]



[Drawing 4]



[Drawing 5]



[Translation done.]

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CORRECTION OR AMENDMENT

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23/12	D
23/14	C

[Procedure revision]
 [Filing Date] August 17, Heisei 10
 [Procedure amendment 1]
 [Document to be Amended] Specification
 [Item(s) to be Amended] Claim
 [Method of Amendment] Modification
 [Proposed Amendment]
 [Claim(s)]
 [Claim 1] The process which forms the 1st base which has a nonvesicular single crystal half conductor layer on the porosity semi-conductor layer on a nonvesicular substrate,
 The lamination process which sticks said nonvesicular single crystal half conductor layer with the 2nd base,
 The separation process which separates said 1st and 2nd stuck bases in said porosity semi-conductor layer,

The production approach of the semi-conductor substrate characterized by having the process which removes the porosity semi-conductor layer allotted on the 2nd [said] base obtained according to said separation process, and the process which removes the porosity semi-conductor layer which constitutes said 1st base obtained according to said separation process.

[Claim 2] The process which forms the 1st base which has a nonvesicular single crystal half conductor layer on the porosity semi-conductor layer on a nonvesicular substrate,

The lamination process which sticks said nonvesicular single crystal half conductor layer through the 2nd base and insulating layer,

The separation process which separates said 1st and 2nd stuck bases in said porosity semi-conductor layer,

The production approach of the semi-conductor substrate characterized by having the process which removes the porosity semi-conductor layer allotted on the 2nd [said] base obtained according to said separation process, and the process which removes the porosity semi-conductor layer which constitutes said 1st base obtained according to said separation process.

[Claim 3] Said porosity semi-conductor layer is the production approach of claim 1 constituted using silicon, or a semi-conductor substrate given in 2.

[Claim 4] The production approach of claim 1 by which the thermal oxidation film is formed in the wall of the hole of said porosity semi-conductor layer, or a semi-conductor substrate given in two.

[Claim 5] Said porosity semi-conductor layer is the production approach of claim 1 which is a layer with a mechanical strength weaker than said nonvesicular substrate, or a semi-conductor substrate given in two.

[Claim 6] The porosity of said porosity semi-conductor layer is the production approach of claim 1 in 10 - 80% of range, or a semi-conductor substrate given in 2.

[Claim 7] Said porosity semi-conductor layer is the production approach of claim 1 which has the two-layer field where porosity differs mutually, or a semi-conductor substrate given in two.

[Claim 8] The two-layer field where said porosity differs is the production approach of a semi-conductor substrate according to claim 7 with the porosity of the side near said nonvesicular substrate higher than the porosity of the side near said nonvesicular single crystal half conductor layer.

[Claim 9] The production approach of claim 1 which performs the process after said lamination process as the 1st base which newly forms a porosity semi-conductor layer in the base which removes the porosity semi-conductor layer which constitutes said 1st base after said separation process, and is obtained, and has said porosity semi-conductor layer for this in it, or a semi-conductor substrate given in 2.

[Claim 10] Said nonvesicular single crystal half conductor layer is the production approach of claim 1 which is Si layer, or a semi-conductor substrate given in 2.

[Claim 11] Said nonvesicular single crystal half conductor layer is the production approach of claim 1 which is a compound semiconductor layer, or a semi-conductor substrate given in 2.

[Claim 12] Said nonvesicular single crystal half conductor layer is the production approach of claim 1 formed of epitaxial growth, or a semi-conductor substrate given in two.

[Claim 13] Said nonvesicular single crystal half conductor layer is the production approach of claim 1 formed by the approach chosen from the molecular-beam epitaxial method, a plasma-CVD method, a reduced pressure CVD method, an optical CVD method, a bias sputtering technique, and a liquid phase grown method, or a semi-conductor substrate given in two.

[Claim 14] Said 1st base is the production approach of claim 1 constituted using Si, or a semi-conductor substrate given in 2.

[Claim 15] Said 2nd base is the production approach of claim 1 which is a light transmission nature base, or a semi-conductor substrate given in 2.

[Claim 16] Removal of said porosity semi-conductor layer is the production approach of claim 1 made using etching, or a semi-conductor substrate given in 2.

[Claim 17] Removal of said porosity semi-conductor layer is the production approach of claim 1 made by grinding alternatively said nonvesicular single crystal half conductor layer for said porosity semi-

conductor layer as a stopper, or a semi-conductor substrate given in 2.

[Claim 18] Removal of said porosity semi-conductor layer is the production approach of claim 1 removed by chemical etching at fluoric acid or fluoric acid by the mixed liquor of alcohol and hydrogen peroxide solution which added either at least, or a semi-conductor substrate given in two.

[Claim 19] Said porosity semi-conductor layer is the production approach of claim 1 removed by chemical etching at buffered fluoric acid or buffered fluoric acid by the mixed liquor of alcohol and hydrogen peroxide solution which added either at least, or a semi-conductor substrate given in two.

[Claim 20] The separation in said porosity semi-conductor layer is the production approach of claim 1 performed by at least one or more approaches of pressurizing in the perpendicular direction to the lamination side of the stuck base, pulling in the direction perpendicular to said field, and applying-to this lamination side-shearing stress **, or a semi-conductor substrate given in 2.

[Claim 21] Said insulating layer is the production approach of the semi-conductor substrate according to claim 2 formed at least in one side on the front face of said 2nd base on said nonvesicular single crystal layer.

[Claim 22] Said insulating layer is the thermal oxidation film and deposition SiO₂. The film and deposition Si₃N₄ The production approach of the semi-conductor substrate according to claim 21 chosen from film.

[Claim 23] Said lamination process is the production approach of the semi-conductor substrate according to claim 1 or 2 performed by anode plate junction, pressurization, heat treatment, or the approach chosen from such combination.

[Claim 24] Said porosity semi-conductor layer is the production approach of the semi-conductor substrate according to claim 1 or 2 formed using anodization.

[Claim 25] Said anodization is the production approach of the semi-conductor substrate according to claim 24 performed in HF solution.

[Claim 26] Said anodization is the production approach of the semi-conductor substrate according to claim 24 performed according to the process which carries out anodization by the low current consistency, and the process which carries out anodization with high current density after that.

[Claim 27] The production approach of a semi-conductor substrate according to claim 26 with the concentration of HF in the process which carries out anodization by said low current consistency deeper than the concentration of HF in the process which carries out anodization with said high current density.

[Claim 28] The separation in said porosity semi-conductor layer is the production approach of claim 1 performed by impressing wave energy to this porosity semi-conductor layer, or a semi-conductor substrate given in 2.

[Claim 29] The separation in said porosity semi-conductor layer is the production approach of claim 1 performed by inserting the member for exfoliation from this porosity semi-conductor layer side face, or a semi-conductor substrate given in 2.

[Claim 30] The separation in said porosity semi-conductor layer is the production approach of claim 1 performed by the expansion energy of the matter into which this porosity semi-conductor layer was infiltrated, or a semi-conductor substrate given in 2.

[Claim 31] The separation in said porosity semi-conductor layer is the production approach of claim 1 performed by the selective etching to this porosity semi-conductor layer of a wafer side face, or a semi-conductor substrate given in 2.

[Claim 32] The semi-conductor substrate produced by the approach according to claim 1 to 31.

[Procedure amendment 2]

[Document to be Amended] Specification

[Item(s) to be Amended] 0032

[Method of Amendment] Modification

[Proposed Amendment]

[0032] Namely, the 1st mode of the production approach of the semi-conductor substrate of this invention The process which forms the 1st base which has a nonvesicular single crystal half conductor layer on the porosity semi-conductor layer on a nonvesicular substrate, The lamination process which

sticks said nonvesicular single crystal half conductor layer with the 2nd base, The separation process which separates said 1st and 2nd stuck bases in said porosity semi-conductor layer, It is characterized by having the process which removes the porosity semi-conductor layer allotted on the 2nd [said] base obtained according to said separation process, and the process which removes the porosity semi-conductor layer which constitutes said 1st base obtained according to said separation process.

[Procedure amendment 3]

[Document to be Amended] Specification

[Item(s) to be Amended] 0033

[Method of Amendment] Modification

[Proposed Amendment]

[0033] The process at which the 2nd mode of this invention forms the 1st base which has a nonvesicular single crystal half conductor layer on the porosity semi-conductor layer on a nonvesicular substrate, The lamination process which sticks said nonvesicular single crystal half conductor layer through the 2nd base and insulating layer, The separation process which separates said 1st and 2nd stuck bases in said porosity semi-conductor layer, It is characterized by having the process which removes the porosity semi-conductor layer allotted on the 2nd [said] base obtained according to said separation process, and the process which removes the porosity semi-conductor layer which constitutes said 1st base obtained according to said separation process.

[Procedure amendment 4]

[Document to be Amended] Specification

[Item(s) to be Amended] 0076

[Method of Amendment] Modification

[Proposed Amendment]

[0076] Next, a substrate is divided in the porosity Si layer 42 (drawing 4 (d)). A light transmission nature support substrate side serves as structure like the 45/light transmission nature support substrate 44 of 43/insulating layers of porosity Si₄₂/single crystal compound semiconductor layers.

[Procedure amendment 5]

[Document to be Amended] Specification

[Item(s) to be Amended] 0166

[Method of Amendment] Modification

[Proposed Amendment]

[0166] This SiO₂ 500nm SiO₂ prepared apart from the layer front face Superposition and after making it contact, heat treatment of 900 degrees C - 2 hours was carried out for the front face of Si substrate in which the layer was formed, and lamination was performed. Subsequently, when the stuck substrate was put in into the tub which arranged the ultrasonic vibrator and ultrasonic energy was impressed, the porosity Si layer broke, the wafer was halved and Porosity Si expressed it.

[Procedure amendment 6]

[Document to be Amended] Specification

[Item(s) to be Amended] 0151

[Method of Amendment] Modification

[Proposed Amendment]

[0151] That is, the single crystal Si layer which had the thickness of 0.3 micrometers on Si oxide film has been formed. It was changeless in a single crystal Si layer in any way also by the selective etching of Porosity Si.

[Procédure amendment 7]

[Document to be Amended] Specification

[Item(s) to be Amended] 0204

[Method of Amendment] Modification

[Proposed Amendment]

[0204] That is, the single crystal Si layer which had the thickness of 0.3 micrometers on Si oxide film has been formed. It was changeless in a single crystal Si layer in any way also by the selective etching of

Porosity Si.

[Translation done.]

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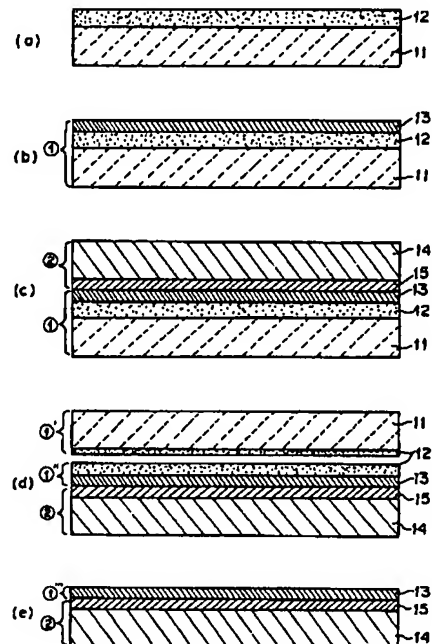
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(33) 優先権主張国	日本 (J P)		

(54) 【発明の名称】 半導体基板の作製方法

(57) 【要約】

【目的】 光透過性基板等の絶縁性基板上に、結晶性が単結晶ウェハ一並に優れたS iあるいは化合物半導体単結晶層を得るうえで、生産性、均一性、制御性、コストの面において卓越した半導体基板の作製方法を提案する。

【構成】 多孔質層12を有する第1の基体11の前記多孔質層12上に非多孔質単結晶半導体層13を形成する工程(a)、(b)、前記非多孔質単結晶半導体層13を第2の基体(14、15)と貼り合わせる工程(c)、前記貼り合わせて構成された基体を前記多孔質層12において分離する工程(d)、前記分離された第2の基体(14、15、13)上に配された多孔質層12を除去する工程(e)、及び前記分離された第1の基体11を構成する多孔質層12を除去する工程を有することを特徴とする半導体基板の作製方法。



【特許請求の範囲】

【請求項 1】 多孔質層を有する第 1 の基体の前記多孔質層上に非多孔質単結晶半導体層を形成する工程、前記非多孔質単結晶半導体層を第 2 の基体と貼り合わせる工程、

前記貼り合わせて構成された基体を前記多孔質層において分離する工程、

前記分離された第 2 の基体上に配された多孔質層を除去する工程、及び前記分離された第 1 の基体を構成する多孔質層を除去する工程を有することを特徴とする半導体基板の作製方法。

【請求項 2】 多孔質層を有する第 1 の基体の前記多孔質層上に非多孔質単結晶半導体層を形成する工程、前記非多孔質単結晶半導体層を第 2 の基体と絶縁層を介して貼り合わせる工程、

前記貼り合わせて構成された基体を前記多孔質層において分離する工程、

前記分離された第 2 の基体上に配された多孔質層を除去する工程、及び前記分離された第 1 の基体を構成する多孔質層を除去する工程を有することを特徴とする半導体基板の作製方法。

【請求項 3】 前記多孔質層は、シリコンを用いて構成される請求項 1 あるいは請求項 2 に記載の半導体基板の作製方法。

【請求項 4】 前記分離された第 1 の基体を構成する多孔質層を除去して得られる基体に、新たに多孔質層を形成し、これを前記多孔質層を有する第 1 の基体として前記貼り合わせ工程以降の工程を行なう請求項 1 あるいは請求項 2 に記載の半導体基板の作製方法。

【請求項 5】 前記非多孔質単結晶半導体層は、Si 層である請求項 1 あるいは 2 に記載の半導体基板の作製方法。

【請求項 6】 前記非多孔質単結晶半導体層は、化合物半導体層である請求項 1 あるいは 2 に記載の半導体基板の作製方法。

【請求項 7】 前記第 1 の基体は、Si を用いて構成される請求項 1 あるいは 2 に記載の半導体基板の作製方法。

【請求項 8】 前記第 2 の基体は、光透過性基体である請求項 1 あるいは 2 に記載の半導体基板の作製方法。

【請求項 9】 前記多孔質層の除去はエッチングを用いてなされる請求項 1 あるいは 2 に記載の半導体基板の作製方法。

【請求項 10】 前記多孔質層の除去は、前記多孔質層を前記非多孔質単結晶半導体層をストッパーとして選択的に研磨することによりなされる請求項 1 あるいは 2 に記載の半導体基板の作製方法。

【請求項 11】 前記多孔質層における分離は、貼り合わせた基体の貼り合わせ面に対して垂直な方向に加圧すること、前記面に垂直な方向に引っ張ること、該貼合

せ面に対して剪断応力をかけること、の少なくとも 1 つ以上の方法によって行われる請求項 1 あるいは 2 に記載の半導体基板の作製方法。

【請求項 12】 前記絶縁層は、前記非多孔質単結晶層上、前記第 2 の基体の表面上の少なくとも一方に形成する請求項 2 に記載の半導体基板の作製方法。

【請求項 13】 前記絶縁層は、熱酸化膜、堆積 SiO₂ 膜、堆積 Si₃N₄ 膜の中から選ばれる請求項 12 に記載の半導体基板の作製方法。

10 【請求項 14】 前記貼り合わせ工程は、陽極接合、加圧、熱処理、あるいはこれらの組み合わせの中から選ばれた方法により行われる請求項 1 又は 2 に記載の半導体基板の作製方法。

【請求項 15】 前記多孔質層は、陽極化成を用いて形成される請求項 1 又は 2 に記載の半導体基板の作製方法。

【請求項 16】 前記陽極化成は、HF 溶液中で行われる請求項 15 に記載の半導体基板の作製方法。

20 【請求項 17】 前記多孔質層における分離は、該多孔質層に波動エネルギーを印加することにより行われる請求項 1 あるいは 2 に記載の半導体基板の作製方法。

【請求項 18】 前記多孔質層における分離は、該多孔質層側面から剥離用部材を挿入することにより行われる請求項 1 あるいは 2 に記載の半導体基板の作製方法。

【請求項 19】 前記多孔質層における分離は、該多孔質層に染み込ませた物質の膨張エネルギーにより行われる請求項 1 あるいは 2 に記載の半導体基板の作製方法。

【請求項 20】 前記多孔質層における分離は、ウェハ側面の該多孔質層に対する選択エッチングにより行われる請求項 1 あるいは 2 に記載の半導体基板の作製方法。

30 【請求項 21】 前記多孔質層の多孔度は、10～80% の範囲にある請求項 1 あるいは 2 に記載の半導体基板の作製方法。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は、半導体基板の作製方法に関する。更に詳しくは、誘電体分離あるいは、絶縁物上の単結晶半導体、半導体基板上の単結晶化合物半導体の作製方法、さらに単結晶半導体層に作成される電子デバイス、集積回路に適する半導体基板の作製方法に関するものである。

【0002】

【従来の技術】絶縁物上の単結晶 Si 半導体層の形成は、シリコン オン インシュレーター (SOI) 技術として広く知られ、通常の Si 集積回路を作製するバルク Si 基板では到達しえない数々の優位点を SOI 技術を利用したデバイスが有することから多くの研究が成されてきた。すなわち、SOI 技術を利用することで、

1. 誘電体分離が容易に高集積化が可能、
2. 対放射線耐性に優れている、
3. 浮遊容量が低減され高速化が可能、

4. ウェル工程が省略できる、
5. ラッチアップを防止できる、
6. 薄膜化による完全空乏型電界効果トランジスタが可能、等の優位点を得られる。

【0003】上記したようなデバイス特性上の多くの利点を実現するために、ここ数十年に渡り、SOI構造の形成方法について研究されてきている。この内容は、例えば以下の文献にまとめられている。

【0004】Special Issue: "Single-crystal silicon on non-single-crystal insulators"; edited by G. W. Cullen, Journal of Crystal Growth, volume 63, no3, pp429~590 (1983). また、古くは、単結晶サファイア基板上に、SiをCVD(化学気相法)で、ヘテロエピタキシーさせて形成するSOS(シリコン オン サファイア)が知られており、最も成熟したSOI技術として一応の成功は収めはしたが、Si層と下地サファイア基板界面の格子不整合により大量の結晶欠陥、サファイア基板からのアルミニウムのSi層への混入、そして何よりも基板の高価格と大面積化への遅れにより、その応用の広がりが妨げられている。比較的近年には、サファイア基板を使用せずにSOI構造を実現しようという試みが行なわれている。この試みは、次の二つに大別される。

【0005】1. Si単結晶基板を表面酸化後に、窓を開けてSi基板を部分的に表出させ、その部分をシードとして横方向へエピタキシャル成長させ、SiO₂上へSi単結晶層を形成する。(この場合には、SiO₂上にSi層の堆積をとまなう。)

2. Si単結晶基板そのものを活性層として使用し、その下部にSiO₂を形成する。(この方法は、Si層の堆積をとまなわない。)また、化合物半導体上のデバイスはSiでは得られない高い性能、たとえば、高速、発光など、を持っている。現在は、これらのデバイスはほとんどGaAs等の化合物半導体基板上にエピタキシャル成長をしてその中に作り込まれている。

【0006】しかし、化合物半導体基板は、高価で、機械的強度が低く、大面積ウェハは作成が困難などの問題点がある。

【0007】このようなことから、安価で、機械的強度も高く、大面積ウェハが作製できるSiウェハ上に、化合物半導体をヘテロエピタキシャル成長させる試みがなされている。

【0008】

【発明が解決しようとしている課題】上記1を実現する手段として、CVDにより、直接、単結晶層Siを横方向エピタキシャル成長させる方法、非晶質Siを堆積して、熱処理により固相横方向エピタキシャル成長させる方法、非晶質あるいは、多結晶Si層に電子線、レーザ

ー光等のエネルギービームを収束して照射し、熔融再結晶により単結晶層をSiO₂上に成長させる方法、そして、棒状ヒーターにより帯状に熔融領域を走査する方法(Zone Melting Recrystallization)が知られている。これらの方法にはそれぞれ一長一短があるが、その制御性、生産性、均一性、品質に多大の問題を残しており、いまだに、工業的に実用化したものはない。たとえば、CVD法は平坦薄膜化するには、犠牲酸化が必要となり、固相成長法ではその結晶性が悪い。また、ビームアニール法では、収束ビーム走査による処理時間と、ビームの重なり具合、焦点調整などの制御性に問題がある。このうち、Zone Melting Recrystallization法がもっとも成熟しており、比較的大規模な集積回路も試作されているが、依然として、亜粒界等の結晶欠陥は、多数残留しており、少数キャリアーデバイスを作成するにいたってない。

【0009】上記2の方法であるSi基板をエピタキシャル成長の種子として用いない方法に於いては、次の4種類の方法が挙げられる。

【0010】1. V型の溝が表面に異方性エッチングされたSi単結晶基板に酸化膜を形成し、該酸化膜上に多結晶Si層をSi基板と同じ程度厚く堆積した後、Si基板の裏面から研磨によって、厚い多結晶Si層上にV溝に囲まれて誘電分離されたSi単結晶領域を形成する。この手法に於ては、結晶性は、良好であるが、多結晶Siを数百ミクロンも厚く堆積する工程、単結晶Si基板を裏面より研磨して分離したSi活性層のみを残す工程に、制御性と生産性の点から問題がある。

【0011】2. サイモックス(SIMOX: Separation by ion implanted oxygen)と称されるSi単結晶基板中に酸素のイオン注入によりSiO₂層を形成する方法であり、Siプロセスと整合性が良いため現在もっとも成熟した手法である。しかしながら、SiO₂層を形成するためには、酸素イオンを 10^{18} ions/cm²以上も注入する必要があるが、その注入時間は長大であり、生産性は高いとはいえず、また、ウェハークストは高い。更に、結晶欠陥は多く残存し、工業的に見て、少数キャリアーデバイスを作製できる十分な品質に至っていない。

【0012】3. 多孔質Siの酸化による誘電体分離によりSOI構造を形成する方法。この方法は、P型Si単結晶基板表面にN型Si層をプロトンイオン注入、(イマイ他, J. Crystal Growth, vol 63, 547 (1983)), もしくは、エピタキシャル成長とパターニングによって島状に形成し、表面よりSi島を囲むようにHF溶液中の陽極化法によりP型Si基板のみを多孔質化したのち、増速酸化によりN型Si島を誘電体分離する方法である。本方法では、分離されているSi領域は、デバイス工程のまえに決定

されており、デバイス設計の自由度を制限する場合があるという問題点がある。

【0013】また、上記のような従来のSOIの形成方法とは別に、近年、Si単結晶基板を、熱酸化した別のSi単結晶基板に、熱処理又は接着剤を用いて張り合せ、SOI構造を形成する方法が注目を浴びている。この方法は、デバイスのための活性層を均一に薄膜化する必要がある。すなわち、数百ミクロンもの厚さのSi単結晶基板をミクロンオーダーかそれ以下に薄膜化する必要がある。この薄膜化には以下のように2種類の方法がある。

【0014】1. 研磨による薄膜化

2. 選択エッチングによる薄膜化

1の研磨では均一に薄膜化することが困難である。特にサブミクロンの薄膜化は、ばらつきが数十%にもなってしまう、この均一化は大きな問題となっている。さらにウェハの大口径化が進めばその困難度は増すばかりである。

【0015】また、2のエッチングは均一な薄膜化に有効とされているが、

- ・せいぜい 10^2 と選択比が充分でない
- ・エッチング後の表面性が悪い

・イオン注入、高濃度Bドーパシ層上のエピタキシャル成長あるいはヘテロエピタキシャル成長を用いているためSOI層の結晶性が悪い等の問題点がある (C. Harendt, et. al., J. Elect. Mater. Vol. 20, 267 (1991), H. Baumgart, et. al., Extended Abstract of ECS 1st International Symposium of Wafer Bonding, pp-733 (1991), C. E. Hunt, Extended Abstract of ECS 1st International Symposium of Wafer Bonding, pp-696 (1991))。

【0016】さらに貼り合わせを用いた半導体基板は、必ず2枚のウェハを必要とし、そのうち1枚はほとんど大部分が研磨・エッチング等により無駄に除去され捨てられてしまい、限りある地球の資源を無駄使いしてしまう。

【0017】したがって、貼り合わせによるSOIにおいては、現状の方法では、その制御性、均一性さらには経済性に多くの問題点が存在する。

【0018】また、ガラスに代表される光透過性基板には、一般には、その結晶構造の無秩序性から、堆積した薄膜Si層は、基板の無秩序性を反映して、非晶質か、良くて多結晶層にしかならず、高性能なデバイスは作製できない。それは、基板の結晶構造が非晶質であることによっており、単に、Si層を堆積しても、良質な単結晶層は得られない。

【0019】ところで、光透過性基板は、光受光素子であるコンタクトセンサーや投影型液晶画像表示装置を構成するうえにおいて重要である。そして、センサーや表示装置の画素(絵素)をより一層、高密度化、高解像度化、高精密化するには、高性能な駆動素子が必要となる。その結果、光透過性基板上に設けられている素子としても優れた結晶性を有する単結晶層を用いて作製されることが必要となる。

【0020】したがって、非晶質Siや多結晶Siでは、その欠陥の多い結晶構造ゆえに要求されるあるいは今後要求されるに十分な性能を持った駆動素子を作製することが難しい。

【0021】上で述べたように、化合物半導体のデバイス作製には化合物半導体の基板が必要不可欠となっている。しかし、化合物半導体の基板は高価で、しかも、大面積化が非常に困難である。

【0022】さらに、Si基板上にGaAs等の化合物半導体をエピタキシャル成長させることが試みられているが、格子定数や熱膨張係数の違いにより、その成長膜は結晶性が悪く、デバイスに応用することは非常に困難となっている。

【0023】また、格子のミスフィットを緩和するため多孔質Si上に化合物半導体をエピタキシャル成長させることが試みられているが、多孔質Siの熱安定性の低さ、経時変化等によりデバイスを作製中あるいは、作製した後の基板としての安定性、信頼性に欠ける。

【0024】こうしたなか、本発明の発明者である米原隆夫は、上述した課題点に鑑み、先に特開平5-21338号公報に開示された新規な半導体部材の製造方法を提案した。

【0025】当該公報に開示された方法は、次のとおりのものである。即ち、多孔質単結晶半導体領域上に非多孔質単結晶半導体領域を配した部材を形成し、前記非多孔質単結晶半導体領域の表面に、表面が絶縁性物質で構成された部材の表面を貼り合わせた後、前記多孔質単結晶半導体領域をエッチングにより除去することを特徴とする半導体部材の製造方法である。

【0026】当該方法は、上述した課題を解決し得る優れたものである。しかしながら、当該公報に開示された方法を更に発展させて半導体基板の生産性の向上、低コスト化が更に図れれば、当該技術分野に係る産業への寄与は極めて大きなものとなる。

【0027】[発明の目的] 本発明は、上述の公報に開示された方法を、更に改善した半導体基板の作製方法を提供することを目的とする。

【0028】本発明の別の目的は、経済性に優れて、大面積に渡り均一平坦な、極めて優れた結晶性を有する単結晶基板を用いて、表面に形成された半導体層あるいは化合物半導体活性層を残して、その片面から該活性層までを取り去り、絶縁物上に欠陥の著しく少ない単結晶層

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あるいは化合物半導体結晶層を得る半導体基板の作製方法を提供することにある。

【0029】本発明の更に別の目的は、透明基板（光透過性基板）上に結晶性が単結晶ウェハ一並に優れたSiあるいは化合物半導体単結晶層を得るうえで、生産性、均一性、制御性、コストの面において卓越した半導体基板の作製方法を提案することにある。

【0030】本発明の更に別の目的は、SOI構造の大規模集積回路を作製する際にも、高価なSOSや、SIMOXの代替足り得る半導体基板の作製方法を提案することにある。

【0031】

【課題を解決するための手段】本発明の半導体基板の作製方法は、下述する構成のものである。

【0032】即ち、本発明の半導体基板の作製方法の第1の態様は、多孔質層を有する第1の基体の前記多孔質層上に非多孔質単結晶半導体層を形成する工程、前記非多孔質単結晶半導体層を第2の基体と貼り合わせる工程、前記貼り合わせて構成された基体を前記多孔質層において分離する工程、前記分離された第2の基体上に配された多孔質層を除去する工程、及び前記分離された第1の基体を構成する多孔質層を除去する工程を有することを特徴とするものである。

【0033】本発明の第2の態様は、多孔質層を有する第1の基体の前記多孔質層上に非多孔質単結晶半導体層を形成する工程、前記非多孔質単結晶半導体層を第2の基体と絶縁層を介して貼り合わせる工程、前記貼り合わせて構成された基体を前記多孔質層において分離する工程、前記分離された第2の基体上に配された多孔質層を除去する工程、及び前記分離された第1の基体を構成する多孔質層を除去する工程を有することを特徴とするものである。

【0034】

【作用】本発明においては、貼り合わせて構成された基体を多孔質層で分離し、非多孔質単結晶半導体層が配された第2の基体上の多孔質層を除去することにより、高品質な非多孔質単結晶半導体層が配された半導体基体を形成できる。これに加えて、貼り合わせて構成された基体を多孔質層で分離し、第1の基体を構成する多孔質層を除去することにより、多孔質層を除去した第1の基体を半導体基板作製に再利用することができる。これにより、半導体基板の生産性の向上、低コスト化が更に図れる。

【0035】本発明によれば、透明基板（光透過性基板）をはじめとする基板上に結晶性が単結晶ウェハ一並に優れたSi等の単結晶層あるいは化合物半導体単結晶層を得るうえで、生産性、均一性、制御性、コストの面において卓越した半導体基板の作製方法を提案することができる。

【0036】また、本発明によれば、SOI構造の大規

模集積回路を作製する際にも、高価なSOSや、SIMOXの代替足り得る半導体基板の作製方法を提案することができる。

【0037】本発明においては、多孔質層を介して基体を2つ以上に分離することができ、分離後の一方の基体は、残留多孔質を除去した後、半導体基板として使用可能であり、他方の基体は、残留多孔質を除去した後、再度、半導体基板の作製に利用することができる。

【0038】本発明においては、基体の両面に多孔質層および非多孔質単結晶層を形成し、該単結晶層を挟むように2枚の別の基体を貼り合わせた後、前記多孔質層で基体を分離することにより同時に2枚の半導体基板を作製することができる。

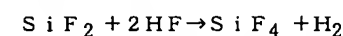
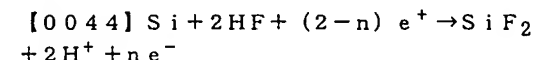
【0039】本発明の半導体基板の作製方法をシリコンを例に挙げて以下に詳細に説明する。

【0040】多孔質Siの機械的強度はporosityにより異なるが、バルクSiよりも十分に弱いと考えられる。たとえば、porosityが50%であれば機械的強度はバルクの半分と考えて良い。すなわち、貼り合わせウェハに圧縮、引っ張りあるいは剪断力をかけると、まず多孔質Si層が破壊されることになる。また、porosityを増加させればより弱い力で多孔質層を破壊できる。

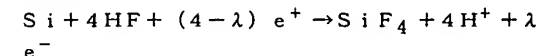
【0041】Si基板はHF溶液を用いた陽極化成法によって多孔質化させることができる。この多孔質Si層は、単結晶Siの密度 2.33 g/cm^3 に比べて、HF溶液濃度を50~20%に変化させることでその密度を $1.1\sim0.6\text{ g/cm}^3$ の範囲に変化させることができる。この多孔質層は、下記の理由により、N型Si層には形成されず、P型Si基板のみに形成される。この多孔質Si層は、透過電子顕微鏡による観察によれば、平均約600オングストローム程度の径の孔が形成される。

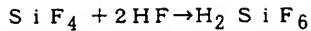
【0042】多孔質Siは、Uhlir等によって1956年に半導体の電解研磨の研究過程において発見された(A. Uhlir, Bell Syst. Tech. J., vol. 35, 333 (1956))。

【0043】また、ウナガミ等は陽極化成におけるSiの溶解反応を研究し、HF溶液中のSiの陽極反応には正孔が必要であり、その反応は、次のようであると報告している(T. ウナガミ, J. Electrochem. Soc., vol. 127, 476 (1980))。



または、





ここで、 e^+ および e^- はそれぞれ正孔と電子を表している。また、 n および λ はそれぞれ Si 原子が溶解するために必要な正孔の数であり、 $n > 2$ または $\lambda > 4$ なる条件が満たされる場合に多孔質 Si が形成されるとしている。

【0045】以上のことから、正孔の存在する P 型 Si は多孔質化されるが、N 型 Si は多孔質化されない。この多孔質化における選択性は長野等および今井によって実証されている（長野、中島、安野、大中、梶原、電子通信学会技術研究報告、vol. 79, SSD79-9549 (1979)）、(K. Imai, Solid-State Electronics, vol. 24, 159 (1981))。

【0046】しかし、高濃度 N 型 Si であれば多孔質化されるとの報告もあり (R. P. Holmstrom and J. Y. Chi, Appl. Phys. Lett., vol. 42, 386 (1983))、P 型、N 型の別にこだわらず、多孔質化を実現できる基板を選ぶことが重要である。

【0047】多孔質 Si 層には、透過電子顕微鏡による観察によれば、平均約 600 オングストローム程度の径の孔が形成されており、その密度は単結晶 Si に比べると、半分以下になるにもかかわらず、単結晶性は維持されており、多孔質層の上部へ単結晶 Si 層をエピタキシャル成長させることも可能である。ただし、1000℃ 以上では、内部の孔の再配列が起こり、増速エッチングの特性が損なわれる。このため、Si 層のエピタキシャル成長には、分子線エピタキシャル成長、プラズマ CVD、減圧 CVD 法、光 CVD、バイアス・スパッター

法、液相成長法等の低温成長が好適とされている。

【0048】また、多孔質層はその内部に大量の空隙が形成されている為に、密度が半分以下に減少する。その結果、体積に比べて表面積が飛躍的に増大するため、その化学エッチング速度は、通常の単結晶層のエッチング速度に比べて、著しく増速される。

【0049】【実施態様例 1】図 1 (a) に示すように、まず第 1 の Si 単結晶基板 11 を用意して、その表面層を多孔質化 12 し、多孔質 Si 12 上に非多孔質単結晶 Si 層 13 を形成する (図 1 (b))。

【0050】次に、図 1 (c) に示すように、もう一方の Si 支持基板 14 と単結晶 Si 層 13 とを絶縁層 15 を介して室温で密着させた後、陽極接合、加圧、あるいは熱処理、あるいはこれらの組み合わせにより貼り合わせる。これにより、Si 支持基板 14 と単結晶層 13 とは絶縁層 15 を介して強固に結合する。絶縁層 15 は単結晶 Si 層上、Si 支持基板 14 上の少なくとも一方に形成する、あるいは絶縁性の薄板をはさみ 3 枚重ねて貼り合わせる。

【0051】次に、多孔質 Si 層 12 で基板を分離する

(図 1 (d))。Si 支持基板側は、多孔質 Si 12 / 単結晶 Si 層 13 / 絶縁層 15 / Si 支持基板 14 のような構造となる。

【0052】さらに、多孔質 Si 12 を選択的に除去する。通常の Si のエッチング液、あるいは多孔質 Si の選択エッチング液である弗酸、あるいは弗酸にアルコールおよび過酸化水素水の少なくともどちらか一方を添加した混合液、あるいは、バッファード弗酸あるいはバッファード弗酸にアルコールおよび過酸化水素水の少なくともどちらか一方を添加した混合液の少なくとも 1 種類を用いて、多孔質 Si 12 のみを無電解湿式化学エッチングして絶縁性基板 15 + 14 上に薄膜化した単結晶 Si 層 13 を残存させ形成する。上記詳述したように、多孔質 Si の膨大な表面積により通常の Si のエッチング液でも選択的に多孔質 Si のみをエッチングすることが可能である。

【0053】あるいは、単結晶 Si 層 13 を研磨ストッパーとして多孔質 Si 12 を選択研磨で除去する。

【0054】図 1 (e) には、本発明で得られる半導体基板が示される。絶縁性基板 15 + 14 上に単結晶 Si 層 13 が平坦に、しかも均一に薄膜化されて、ウェハ全域に、大面積に形成される、こうして得られた半導体基板は、絶縁分離された電子素子作製という点から見ても好適に使用することができる。

【0055】第 1 の Si 単結晶基板 11 は、残留多孔質 Si を除去して、表面平坦性が許容できないほど荒れている場合には、表面平坦化を行なった後、再度第 1 の Si 単結晶基板 11 として使用する。

【0056】本発明において、多孔質 Si 層で 2 つの基体を分離する方法としては、貼り合わせた基体の両側より加圧して多孔質層を押しつぶす方法、それぞれの基体を両側に引き、両者を分離する方法、多孔質層に治具をそう入する方法、貼り合わせた基体の表面に平行な方向に力を加える方法、多孔層に超音波振動を加える方法等が採用できる。

【0057】本発明において、分離に適した多孔質 Si 層の多孔度 (porosity) は、一般的には 10 ~ 80 % の範囲であり、より好ましくは、20 ~ 60 % の範囲である。

【0058】【実施態様例 2】図 2 (a) に示すように、まず第 1 の Si 単結晶基板 21 を用意して、その表面層を多孔質化 22 し、多孔質 Si 22 上に非多孔質単結晶 Si 層 23 を形成する (図 2 (b))。

【0059】次に、図 2 (c) に示すように、石英やガラスに代表される光透過性支持基板 24 と単結晶 Si 層 23 とを絶縁層 25 を介して室温で密着させた後、陽極接合、加圧、あるいは熱処理、あるいはこれらの組み合わせにより貼り合わせる。これにより、光透過性支持基板 24 と単結晶層 23 とは絶縁層 25 を介して強固に結合する。絶縁層 25 は単結晶 Si 層上、光透過性支持基

板24上の少なくとも一方に形成する、あるいは絶縁性の薄板をはさみ3枚重ねて貼り合わせる。

【0060】次に、多孔質Si層23で基板を分割する(図2(d))。光透過性支持基板側は、多孔質Si22/単結晶Si層23/絶縁層25/光透過性支持基板24のような構造となる。

【0061】さらに、多孔質Si22を選択的に除去する。通常のSiのエッチング液、あるいは多孔質Siの選択エッチング液である弗酸、あるいは弗酸にアルコールおよび過酸化水素水の少なくともどちらか一方を添加した混合液、あるいは、バッファード弗酸あるいはバッファード弗酸にアルコールおよび過酸化水素水の少なくともどちらか一方を添加した混合液の少なくとも1種類を用いて、多孔質Si22のみを無電解湿式化学エッチングして光透過性絶縁性基板25+24上に薄膜化した単結晶Si層23を残存させ形成する。上記詳述したように、多孔質Siの膨大な表面積により通常のSiのエッチング液でも選択的に多孔質Siのみをエッチングすることが可能である。

【0062】あるいは、単結晶Si層23を研磨ストッパーとして多孔質Si22を選別研磨で除去する。

【0063】図2(e)には、本発明で得られる半導体基板が示される。光透過性絶縁性基板25+24上に単結晶Si層23が平坦に、しかも均一に薄膜化されて、ウェハ全域に、大面積に形成される。こうして得られた半導体基板は、絶縁分離された電子素子作製という点から見ても好適に使用することができる。

【0064】絶縁在層25はなくても良い。

【0065】第1のSi単結晶基板21は、残留多孔質Siを除去して、表面平坦性が許容できないほど荒れている場合には、表面平坦化を行なった後、再度第1のSi単結晶基板21として使用できる。

【0066】[実施態様例3]図3(a)に示すように、まず第1のSi単結晶基板31を用意して、その表面層を多孔質化42し、多孔質Si32上に非多孔質単結晶化合物半導体層33を形成する(図3(b))。

【0067】次に、図3(c)に示すように、もう一方のSi支持基板34と単結晶化合物半導体層33とを絶縁層35を介して室温で密着させた後、陽極接合、加圧、あるいは熱処理、あるいはこれらの組み合わせにより貼り合わせる。これにより、Si支持基板34と単結晶層33とは絶縁層35を介して強固に結合する。絶縁層35は単結晶化合物半導体層上、Si支持基板34上の少なくとも一方に形成する、あるいは絶縁性の薄板をはさみ3枚重ねて貼り合わせる。

【0068】次に、多孔質Si層32で基板を分割する(図3(d))。Si支持基板側は、多孔質Si32/単結晶化合物半導体層33/絶縁層35/Si支持基板34のような構造となる。

【0069】さらに、多孔質Si32を選択的に除去す

る。化合物半導体に対してSiのエッチング速度の早いエッチング液を用いて、多孔質Si32のみを化学エッチングして絶縁性基板35+34上に薄膜化した単結晶化合物半導体層33を残存させ形成する。

【0070】あるいは、単結晶化合物半導体層33を研磨ストッパーとして多孔質Si32を選択研磨で除去する。

【0071】図3(e)には、本発明で得られる半導体基板が示される。絶縁性基板35+34上に単結晶化合物半導体層33が平坦に、しかも均一に薄膜化されて、ウェハ全域に、大面積に形成される。こうして得られた半導体基板は、化合物半導体基板として、さらには絶縁分離された電子素子作製という点から見ても好適に使用することができる。

【0072】化合物半導体基板として用いる場合には絶縁層35はなくても良い。

【0073】第1のSi単結晶基板31は、残留多孔質Siを除去して、表面平坦性が許容できないほど荒れている場合には、表面平坦化を行なった後、再度第1のSi単結晶基板31として使用できる。

【0074】[実施態様例4]図4(a)に示すように、まず第1のSi単結晶基板41を用意して、その表面層を多孔質化42し、多孔質Si42上に非多孔質単結晶化合物半導体層43を形成する(図4(b))。

【0075】次に、図4(c)に示すように、石英やガラスに代表される光透過性支持基板44と単結晶化合物半導体層43とを絶縁層45を介して室温で密着させた後、陽極接合、加圧、あるいは熱処理、あるいはこれらの組み合わせにより貼り合わせる。これにより、光透過性支持基板44と単結晶層43とは絶縁層45を介して強固に結合する。絶縁層45は単結晶化合物半導体層上、光透過性支持基板44上の少なくとも一方に形成する、あるいは絶縁性の薄板をはさみ3枚重ねて貼り合わせる。

【0076】次に、多孔質Si層43で基板を分割する(図4(d))。光透過性支持基板側は、多孔質Si42/単結晶化合物半導体層43/絶縁層45/光透過性支持基板44のような構造となる。

【0077】さらに、多孔質Si42を選択的に除去する。化合物半導体に対してSiのエッチング速度の速いエッチング液を用いて、多孔質Si42のみを化学エッチングして絶縁性基板45+44上に薄膜化した単結晶化合物半導体層43を残存させ形成する。

【0078】あるいは、単結晶化合物半導体層43を研磨ストッパーとして多孔質Si42を選別研磨で除去する。

【0079】図4(e)には、本発明で得られる半導体基板が示される。光透過性絶縁性基板45+44上に単結晶化合物半導体層43が平坦に、しかも均一に薄膜化されて、ウェハ全域に、大面積に形成される。こうして

得られた半導体基板は、絶縁分離された電子素子作製という点から見ても好適に使用することができる。

【0080】絶縁介在層45はなくても良い。

【0081】第1のSi単結晶基板41は、残留多孔質Siを除去して、表面平坦性が許容できないほど荒れている場合には、表面平坦化を行なった後、再度第1のSi単結晶基板41として使用できる。

【0082】【実施態様例5】図5(a)に示すように、まず第1のSi単結晶基板51を用意して、その両面の表面層を多孔質化52、53し、両面の多孔質Si52、53上に非多孔質単結晶半導体層54、55を形成する(図5(b))。

【0083】次に、図5(c)に示すように、2枚の支持基板56、57と単結晶半導体層54、55とをそれぞれ絶縁層58、59を介して室温で密着させた後、陽極接合、加圧、あるいは熱処理、あるいはこれらの組み合わせにより貼り合わせる。これにより、支持基板56、57と単結晶層54、55とは絶縁層58、59を介して強固に結合する。絶縁層58、59は単結晶半導体層54、55上、支持基板56、57上の少なくとも一方に形成する、あるいは絶縁性の薄板をはさみ5枚重ねて貼り合わせる。

【0084】次に、両多孔質Si層52、53で基板を三分割する(図5(d))。2枚の支持基板は、多孔質Si/単結晶半導体層/絶縁層/支持基板(52/54/58/56、および53/55/59/57)のような構造となる。

【0085】さらに、両多孔質Si52、53を選択的に除去する。多孔質Si52、53のみを選択的に化学エッチングして支持基板58/56および59/57上に薄膜化した単結晶半導体層54、55を残存させ形成する。

【0086】あるいは、単結晶半導体層54、55を研磨ストッパーとして多孔質Si52、53を選択、研磨で除去する。

【0087】図5(e)には、本発明で得られる半導体基板が示される。支持基板上に単結晶化合物半導体層が平坦に、しかも均一に薄膜化されて、ウェハ全域に、大面積に2体同時に形成される。こうして得られた半導体基板は、絶縁分離された電子素子作製という点から見ても好適に使用することができる。

【0088】絶縁介在層58、59はなくても良い。

【0089】支持基板56、57は同一でなくても良い。

【0090】第1のSi単結晶基板51は、残留多孔質Siを除去して、表面平坦性が許容できないほど荒れている場合には、表面平坦化を行なった後、再度第1のSi単結晶51として使用できる。

【0091】

【実施例】

(実施例1) 625 μ mの厚みを持った比抵抗0.01 $\Omega \cdot \text{cm}$ のP型の6インチ径の第1の(100)単結晶Si基板を、HF溶液中において陽極化成を行った。

【0092】陽極化成条件は以下のとおりであった。

【0093】電流密度: 5($\text{mA} \cdot \text{cm}^{-2}$)

陽極化成溶液: HF:H₂O:C₂H₅OH=1:1:1

時間: 12(分)

多孔質Siの厚み: 10(μ m)

Porosity: 15(%)

この基板を酸素雰囲気中400℃で1時間酸化した。この酸化により多孔質Siの孔の内壁は熱酸化膜で覆われた。多孔質Si上にCVD(Chemical Vapor Deposition)法により単結晶Siを1 μ mエピタキシャル成長した。成長条件は以下の通りである。

【0094】ソースガス: SiH₂Cl₂/H₂

ガス流量: 0.5/180 l/min

ガス圧力: 80 Torr

温度: 950℃

成長速度: 0.3 μ m/min

さらに、このエピタキシャルSi層表面に熱酸化により100nmのSiO₂層を形成した。

【0095】該SiO₂層表面と別に用意した500nmのSiO₂層を形成したSi基板の表面とを重ね合わせ、接触させた後、900℃-2時間の熱処理をし、貼り合わせをおこなった。

【0096】貼り合わせたウェハの面に対して垂直方向に均一に十分な引っ張り力を加えたところ多孔質Si層が破壊しウェハは二分割され、多孔質Siが表出した。具体的には、貼り合わせたウェハの両面にプレートを接着剤を用いて接着し、該プレートを該プレートを互いに引き離す方向に移動せしめる治具に配した後、2つに引き離した。

【0097】その後、多孔質Si層を49%弗酸と30%過酸化水素水との混合液(1:5)で攪拌しながら選択エッチングした。単結晶Siはエッチングされずに残り、単結晶Siをエッチ・ストップの材料として、多孔質Siは選択エッチングされ、完全に除去された。

【0098】非多孔質Si単結晶の該エッチング液に対するエッチング速度は、極めて低く、多孔質層のエッチング速度との選択比は十の五乗以上にも達し、非多孔質層におけるエッチング量(数十オングストローム程度)は実用上無視できる膜厚減少である。

【0099】すなわち、Si酸化膜上に1 μ mの厚みを持った単結晶Si層が形成できた。多孔質Siの選択エッチングによっても単結晶Si層には何ら変化はなかった。

【0100】透過電子顕微鏡による断面観察の結果、Si層には新たな結晶欠陥は導入されておらず、良好な結

晶性が維持されていることが確認された。

【0101】こうして、高品質な半導体層を有するSOI基板が得られた。更に、多孔質Si層を境に分離した他方のSi基板に残存する多孔質層を同様のエッチングにより除去した後、表面をポリッシングした。こうして得られたSi基板を用いて上述の工程を繰り返すことにより高品質な半導体層を有するSOI基板複数個が得られた。

【0102】（実施例2）525 μ mの厚みを持った比抵抗0.01 $\Omega \cdot \text{cm}$ のP型の4インチ径の第1の（100）単結晶Si基板を、HF溶液中において陽極化成を行った。

【0103】陽極化成条件は以下のとおりであった。

【0104】電流密度：7（mA $\cdot \text{cm}^{-2}$ ）

陽極化成溶液：HF：H₂O：C₂H₅OH=1：1：1

時間：12（分）

多孔質Siの厚み：10（ μ m）

Porosity：15（%）

この基板を酸素雰囲気中400℃で2時間酸化した。この酸化により多孔質Siの孔の内壁は熱酸化膜で覆われた。多孔質Si上にMBE（Molecular Beam Epitaxy）法により単結晶Siを0.5 μ mエピタキシャル成長した。成長条件は以下の通りである。

【0105】温度：700℃

圧力：1 $\times 10^{-9}$ Torr

成長速度：0.1nm/sec

温度：950℃

成長速度：0.3 μ m/min

さらに、このエピタキシャルSi層表面に熱酸化により100nmのSiO₂層を形成した。

【0106】該SiO₂層表面と別に用意した熔融石英基板の表面とを重ね合わせ、接触させた後、400℃-2時間の熱処理をし、貼り合わせをおこなった。

【0107】貼り合わせたウェハの面に対して垂直方向に均一に十分な圧力を加えたところ多孔質Si層が破壊しウェハは二分割され、多孔質Siが表出した。具体的には、貼り合わせたウェハの両面にプレートに接着剤を用いて接着し、該プレートを該プレートを実施例1で述べた治具に配した後、該プレートに圧力を加えることでSi層を破壊した。

【0108】その後、多孔質Si層をバッファード弗酸と30%過酸化水素水との混合液（1：5）で攪拌しながら選択エッチングする。単結晶Siはエッチングされずに残り、単結晶Siをエッチ・ストップの材料として、多孔質Siは選択エッチングされ、完全に除去された。

【0109】非多孔質Si単結晶の該エッチング液に対するエッチング速度は、極めて低く、多孔質層のエッチ

ング速度との選択比は十の五乗以上にも達し、非多孔質層におけるエッチング量（数十オングストローム程度）は実用上無視できる膜厚減少である。

【0110】すなわち、熔融石英基板上に0.5 μ mの厚みを持った単結晶Si層が形成できた。多孔質Siの選択エッチングによっても単結晶Si層には何ら変化はなかった。

【0111】透過電子顕微鏡による断面観察の結果、Si層には新たな結晶欠陥は導入されておらず、良好な結晶性が維持されていることが確認された。

【0112】実施例1と同様にして、上述の工程を繰り返すことにより高品質な半導体層を有するSOI基板複数個が得られた。

【0113】（実施例3）625 μ mの厚みを持った比抵抗0.01 $\Omega \cdot \text{cm}$ のP型あるいはN型の6インチ径の第1の（100）単結晶Si基板を、HF溶液中において陽極化成を行った。

【0114】陽極化成条件は以下のとおりであった。

【0115】電流密度：7（mA $\cdot \text{cm}^{-2}$ ）

陽極化成溶液：HF：H₂O：C₂H₅OH=1：1：1

時間：12（分）

多孔質Siの厚み：10（ μ m）

Porosity：15（%）

この基板を酸素雰囲気中400℃で1時間酸化した。この酸化により多孔質Siの孔の内壁は熱酸化膜で覆われた。多孔質Si上にMOCVD（Metal Organic Chemical Vapor Deposition）法により単結晶GaAsを1 μ mエピタキシャル成長した。成長条件は以下の通りである。

【0116】ソースガス：TMG/AsH₃/H₂

ガス圧力：80Torr

温度：700℃

該GaAs層表面と別に用意した第2のSi基板の表面とを重ね合わせ、接触させた後、900℃-1時間の熱処理をし、貼り合わせをおこなった。この熱処理により両基板は強固に貼り合わされた。

【0117】貼り合わせたウェハに実施例2と同様にして圧力を加えたところ多孔質Si層が破壊しウェハは二分割され、多孔質Siが表出した。

【0118】その後、多孔質Si層を内壁の酸化膜を弗酸で除去した後、多孔質Siをエチレンジアミン+ピロカテコール+水（17ml：3g：8mlの比率）110℃でエッチングした。単結晶GaAsはエッチングされずに残り、単結晶GaAsをエッチ・ストップの材料として、多孔質Siは選択エッチングされ、完全に除去された。

【0119】単結晶GaAsの該エッチング液に対するエッチング速度は、極めて低く、実用上無視できる膜厚減少である。

【0120】すなわち、Si基板上に1 μ mの厚みを持った単結晶GaAs層が形成できた。多孔質Siの選択エッチングによっても単結晶GaAs層には何ら変化はなかった。

【0121】透過電子顕微鏡による断面観察の結果、GaAs層には新たな結晶欠陥は導入されておらず、良好な結晶性が維持されていることが確認された。

【0122】実施例2と同様にして、上述の工程を繰り返し、高品質なGaAs層を配した複数の半導体基板が得られた。

【0123】支持基板として酸化膜付きのSi基板を用いることにより、絶縁膜上のGaAsも同様に作製できた。

【0124】(実施例4) 625 μ mの厚みを持った比抵抗0.01 $\Omega \cdot \text{cm}$ のP型あるいはN型の5インチ径の第1の(100)単結晶Si基板を、HF溶液中において陽極化成を行った。

【0125】陽極化成条件は以下のとおりであった。

【0126】電流密度: 10 ($\text{mA} \cdot \text{cm}^{-2}$)

陽極化成溶液: HF: H₂O: C₂H₅OH = 1: 1: 1

時間: 24 (分)

多孔質Siの厚み: 20 (μm)

Porosity: 17 (%)

この基板を酸素雰囲気中400℃で2時間酸化した。この酸化により多孔質Siの孔の内壁は熱酸化膜で覆われた。多孔質Si上にMBE (Molecular Beam Epitaxy) 法により単結晶AlGaAsを0.5 μm エピタキシャル成長した。

【0127】該AlGaAs層表面と別に用意した低融点ガラス基板の表面とを重ね合わせ、接触させた後、500℃-2時間の熱処理をし、貼り合わせをおこなった。この熱処理により両基板は強固に貼り合わされた。

【0128】貼り合わせたウェハ実施例2と同様にして圧力を加えたところ多孔質Si層が破壊しウェハは二分割され、多孔質Siが表出した。

【0129】その後、多孔質Siを弗酸溶液でエッチングした。単結晶AlGaAsはエッチングされずに残り、単結晶AlGaAsをエッチ・ストップの材料として、多孔質Siは選択エッチングされ、完全に除去された。

【0130】単結晶AlGaAsの該エッチング液に対するエッチング速度は、極めて低く、実用上無視できる膜厚減少である。

【0131】すなわち、ガラス基板上に0.5 μm の厚みを持った単結晶AlGaAs層が形成できた。多孔質Siの選択エッチングによっても単結晶AlGaAs層には何ら変化はなかった。

【0132】透過電子顕微鏡による断面観察の結果、AlGaAs層には新たな結晶欠陥は導入されておらず、

良好な結晶性が維持されていることが確認された。実施例2と同様にして、上述の工程を繰り返すことにより高品質な半導体層を有する基板が複数個得られた。

【0133】(実施例5) 625 μm の厚みを持った比抵抗0.01 $\Omega \cdot \text{cm}$ のP型あるいはN型の両面研磨の6インチ径の第1の(100)単結晶Si基板を、HF溶液中において両面に対して陽極化成を行った。

【0134】陽極化成条件は以下のとおりであった。

【0135】電流密度: 5 ($\text{mA} \cdot \text{cm}^{-2}$)

10 陽極化成溶液: HF: H₂O: C₂H₅OH = 1: 1: 1

時間: 12 \times 2 (分)

多孔質Siの厚み: 各10 (μm)

Porosity: 15 (%)

この基板を酸素雰囲気中400℃で1時間酸化した。この酸化により多孔質Siの孔の内壁は熱酸化膜で覆われた。両面に形成した多孔質Si上にCVD (Chemical Vapor Deposition) 法により単結晶Siをそれぞれ1 μm エピタキシャル成長した。成長条件は以下の通りである。

【0136】ソースガス: SiH₂Cl₂/H₂

ガス流量: 0.5/180 l/min

ガス圧力: 80 Torr

温度: 950℃

成長速度: 0.3 $\mu\text{m}/\text{min}$

さらに、このエピタキシャルSi層表面に熱酸化により100nmのSiO₂層を形成した。

【0137】該SiO₂層表面と別に用意した500nmのSiO₂層を形成した2枚のSi基板の表面とをそれぞれ重ね合わせ、接触させた後、600℃-2時間の熱処理をし、貼り合わせをおこなった。

【0138】実施例1の手法を用いて貼り合わせたウェハの面に対して垂直方向に十分な引っ張り力を加えたところ多孔質Si層が2層とも破壊しウェハは三分割され、多孔質Siが表出した。

【0139】その後、多孔質Si層を49%弗酸と30%過酸化水素水との混合液(1:5)で攪拌しながら選択エッチングする。単結晶Siはエッチングされずに残り、単結晶Siをエッチ・ストップの材料として、多孔質Siは選択エッチングされ、完全に除去された。

【0140】非多孔質Si単結晶の該エッチング液に対するエッチング速度は、極めて低く、多孔質層のエッチング速度との選択比は十の五乗以上にも達し、比多孔質層におけるエッチング量(数十オングストローム程度)は実用上無視できる膜厚減少である。

【0141】すなわち、Si酸化膜上に1 μm の厚みを持った単結晶Si層が2枚同時に形成できた。多孔質Siの選択エッチングによっても単結晶Si層には何ら変化はなかった。

【0142】透過電子顕微鏡による断面観察の結果、S

i 層には新たな結晶欠陥は導入されておらず、良好な結晶性が維持されていることが確認された。実施例1と同様に上述の工程を繰り返し、高品質な半導体層を有する基板複数個を得た。

【0143】(実施例6) 625 μm の厚みを持った比抵抗 $0.01 \Omega \cdot \text{cm}$ の P 型あるいは N 型の 5 インチ径の第1の (100) 単結晶 Si 基板を、HF 溶液中において陽極化成を行った。

【0144】陽極化成条件は以下のとおりであった。

【0145】電流密度: 7 ($\text{mA} \cdot \text{cm}^{-2}$)

陽極化成溶液: HF : H₂O : C₂H₅OH = 1 : 1 : 1

時間: 4 (分)

多孔質 Si の厚み: 3 (μm)

Porosity: 15 (%)

さらに

電流密度: 30 ($\text{mA} \cdot \text{cm}^{-2}$)

陽極化成溶液: HF : H₂O : C₂H₅OH = 1 : 3 : 2

時間: 3 (分)

多孔質 Si の厚み: 10 (μm)

Porosity: 45 (%)

この基板を酸素雰囲気中 400℃ で 1 時間酸化した。この酸化により多孔質 Si の孔の内壁は熱酸化膜で覆われた。多孔質 Si 上に CVD 法により単結晶 Si を 0.3 μm エピタキシャル成長した。成長条件は以下の通りである。

【0146】ソースガス: SiH₄

キャリアーガス: H₂

温度: 850℃

圧力: 1×10^{-2} Torr

成長速度: 3.3 nm/sec

さらに、このエピタキシャル Si 層表面に熱酸化により 100 nm の SiO₂ 層を形成した。

【0147】該 SiO₂ 層表面と別に用意した 500 nm の SiO₂ 層を形成した Si 基板の表面とを重ね合わせ、接触させた後、700℃ - 2 時間の熱処理をし、貼り合わせをおこなった。

【0148】実施例1の手法を用いて、貼り合わせたウェハの面に対して垂直方向に十分な引っ張り力を加えたところで多孔質 Si 層が破壊しウェハは二分割され、多孔質 Si が表出した。

【0149】その後、多孔質 Si 層を HF/HNO₃/CH₃COOH 系のエッチング液で選択エッチングする。多孔質 Si はエッチングされ、完全に除去された。

【0150】非多孔質 Si 単結晶の該エッチング液に対するエッチング速度は、極めて低く、非多孔質層におけるエッチング量は実用上無視できる膜厚減少である。

【0151】すなわち、Si 酸化膜上に 1 μm の厚みを持った単結晶 Si 層が形成できた。多孔質 Si の選択エ

ッチングによっても単結晶 Si 層には何ら変化はなかった。

【0152】透過電子顕微鏡による断面観察の結果、Si 層には新たな結晶欠陥は導入されておらず、良好な結晶性が維持されていることが確認された。実施例1と同様に上述の工程を繰り返し、高品質な半導体層を有する基板複数個を得た。

【0153】(実施例7) 625 μm の厚みを持った比抵抗 $0.01 \Omega \cdot \text{cm}$ の P 型あるいは N 型の 6 インチ径の第1の (100) 単結晶 Si 基板を、HF 溶液中において陽極化成を行った。

【0154】陽極化成条件は以下のとおりであった。

【0155】電流密度: 5 ($\text{mA} \cdot \text{cm}^{-2}$)

陽極化成溶液: HF : H₂O : C₂H₅OH = 1 : 1 : 1

時間: 12 (分)

多孔質 Si の厚み: 10 (μm)

Porosity: 15 (%)

この基板を酸素雰囲気中 400℃ で 1 時間酸化した。この酸化により多孔質 Si の孔の内壁は熱酸化膜で覆われた。多孔質 Si 上に CVD (Chemical Vapor Deposition) 法により単結晶 Si を 1 μm エピタキシャル成長した。成長条件は以下の通りである。

【0156】ソースガス: SiH₂Cl₂/H₂

ガス流量: 0.5/180 l/min

ガス圧力: 80 Torr

温度: 950℃

成長速度: 0.3 $\mu\text{m}/\text{min}$

さらに、このエピタキシャル Si 層表面に熱酸化により 100 nm の SiO₂ 層を形成した。

【0157】該 SiO₂ 層表面と別に用意した 500 nm の SiO₂ 層を形成した Si 基板の表面とを重ね合わせ、接触させた後、900℃ - 2 時間の熱処理をし、貼り合わせをおこなった。

【0158】実施例1の手法を用いて、貼り合わせたウェハの面に対して垂直方向に十分な引っ張り力を加えたところ多孔質 Si 層が破壊しウェハは二分割され、多孔質 Si が表出した。

【0159】その後、多孔質 Si 層を単結晶 Si をストッパーとして選択研磨した。多孔質 Si 選択研磨され、完全に除去された。

【0160】すなわち、Si 酸化膜上に 1 μm の厚みを持った単結晶 Si 層が形成できた。多孔質 Si の選択エッチングによっても単結晶 Si 層には何ら変化はなかった。

【0161】透過電子顕微鏡による断面観察の結果、Si 層には新たな結晶欠陥は導入されておらず、良好な結晶性が維持されていることが確認された。実施例1と同様に上述の工程を繰り返し、高品質な半導体層を有

する基板複数個を得た。

【0162】(実施例8) 625 μ mの厚みを持った比抵抗0.01 $\Omega \cdot \text{cm}$ のP型あるいはN型の6インチ径の第1の(100)単結晶Si基板を、HF溶液中において陽極化成を行った。

【0163】陽極化成条件は以下のとおりであった。

【0164】電流密度: 5 (mA $\cdot \text{cm}^{-2}$)

陽極化成溶液: HF: H₂O: C₂H₅OH = 1: 1: 1

時間: 12 (分)

多孔質Siの厚み: 10 (μ m)

Porosity: 15 (%)

この基板を酸素雰囲気中400℃で1時間酸化した。この酸化により多孔質Siの孔の内壁は熱酸化膜で覆われた。多孔質Si上にCVD (Chemical Vapor Deposition) 法により単結晶Siを1 μ mエピタキシャル成長した。成長条件は以下の通りである。

【0165】ソースガス: SiH₂Cl₂/H₂

ガス流量: 0.5/180 l/min

ガス圧力: 80 Torr

温度: 950℃

成長速度: 0.3 μ m/min

さらに、このエピタキシャルSi層表面に熱酸化により100nmのSiO₂層を形成した。

【0166】該SiO₂層表面と別に用意した500nmのSiO₂層を形成したSi基板の表面とを重ね合わせ、接触させた後、900℃-2時間の熱処理をし、貼り合わせをおこなった。次いで貼り合わせた基板を超音波振動子を配した層の中に入れ、超音波エネルギーを印加したところ多孔質Si層が破壊しウェハは二分割され、多孔質Siが表出した。

【0167】その後、多孔質Si層を49%弗酸と30%過酸化水素水との混合液(1:5)で攪はんしながら選択エッチングする。単結晶Siはエッチングされずに残り、単結晶Siをエッチ・ストップの材料として、多孔質Siは選択エッチングされ完全に除去された。

【0168】非多孔質Si単結晶の該エッチング液にたいするエッチング速度は、極めて低く、多孔質層のエッチング速度との選択比は十の五乗以上にも達し、非多孔質層におけるエッチング量(数十オングストローム程度)は実用上無視できる膜厚減少である。

【0169】すなわち、Si酸化膜上に1 μ mの厚みを持った単結晶Si層が形成できた。多孔質Siの選択エッチングによっても単結晶Si層には何ら変化はなかった。

【0170】透過電子顕微鏡による断面観察の結果、Si層には新たな結晶欠陥は導入されておらず、良好な結晶性が維持されていることが確認された。

【0171】第1のSi単結晶基板は残留多孔質Siを

除去して、再度第1のSi単結晶基板として使用した。

【0172】(実施例9) 525 μ mの厚みを持った比抵抗0.01 $\Omega \cdot \text{cm}$ のP型あるいはN型の4インチ径の第1の(100)単結晶Si基板を、HF溶液中において陽極化成を行った。

【0173】陽極化成条件は以下のとおりであった。

【0174】電流密度: 7 (mA $\cdot \text{cm}^{-2}$)

陽極化成溶液: HF: H₂O: C₂H₅OH = 1: 1: 1

10 時間: 12 (分)

多孔質Siの厚み: 10 (μ m)

Porosity: 15 (%)

この基板を酸素雰囲気中400℃で2時間酸化した。この酸化により多孔質Siの孔の内壁は熱酸化膜で覆われた。多孔質Si上にMBE (Molecular Beam Epitaxy) 法により単結晶Siを0.5 μ mエピタキシャル成長した。成長条件は以下の通りである。

【0175】温度: 700℃

20 圧力: 1 $\times 10^{-9}$ Torr

成長速度: 0.1nm/sec

温度: 950℃

成長速度: 0.3 μ m/min

さらに、このエピタキシャルSi層表面に熱酸化により100nmのSiO₂層を形成した。

【0176】該SiO₂層表面と別に用意した熔融石英基板の表面とを重ね合わせ、接触させた後、400℃-2時間の熱処理をし、貼り合わせをおこなった。

【0177】ウェハ端面に多孔質層を表出させ、多孔質Siをある程度エッチングし、そこへ剃刀の刃のように鋭利な板を挿入したところ多孔質Si層が破壊しウェハは二分割され、多孔質Siが表出した。

【0178】その後、多孔質Si層をバッファード弗酸と30%過酸化水素水との混合液(1:5)で攪はんしながら選択エッチングする。単結晶Siはエッチングされずに残り、単結晶Siをエッチ・ストップの材料として、多孔質Siは選択エッチングされ完全に除去された。

【0179】非多孔質Si単結晶の該エッチング液にたいするエッチング速度は、極めて低く、多孔質層のエッチング速度との選択比は十の五乗以上にも達し、非多孔質層におけるエッチング量(数十オングストローム程度)は実用上無視できる膜厚減少である。

【0180】すなわち、熔融石英基板上に0.5 μ mの厚みを持った単結晶Si層が形成できた。多孔質Siの選択エッチングによっても単結晶Si層には何ら変化はなかった。

【0181】透過電子顕微鏡による断面観察の結果、Si層には新たな結晶欠陥は導入されておらず、良好な結晶性が維持されていることが確認された。

【0182】エピタキシャルSi層表面に酸化膜を形成しなくても同様の結果が得られた。

【0183】第1のSi単結晶基板は残留多孔質Siを除去して、表面研磨を行い鏡面状にした後、再度第1のSi単結晶基板として使用した。

【0184】(実施例10) 625 μ mの厚みを持った比抵抗0.01 $\Omega \cdot \text{cm}$ のP型あるいはN型の両面研磨の6インチ径の第1の(100)単結晶Si基板を、HF溶液中において両面に対して陽極化成を行った。

【0185】陽極化成条件は以下のとおりであった。

【0186】電流密度: 5 (mA $\cdot \text{cm}^{-2}$)

陽極化成溶液: HF:H₂O:C₂H₅OH=1:1:1

時間: 12 \times 2 (分)

多孔質Siの厚み: 各10 (μ m)

Porosity: 15 (%)

この基板を酸素雰囲気中400 $^{\circ}\text{C}$ で1時間酸化した。この酸化により多孔質Siの孔の内壁は熱酸化膜で覆われた。両面に形成した多孔質Si上にCVD (Chemical Vapor Deposition) 法により単結晶Siを1 μ mエピタキシャル成長した。成長条件は以下の通りである。

【0187】ソースガス: SiH₂Cl₂/H₂

ガス流量: 0.5/180 l/min

ガス圧力: 80 Torr

温度: 950 $^{\circ}\text{C}$

成長速度: 0.3 μ m/min

さらに、このエピタキシャルSi層表面に熱酸化により100nmのSiO₂層を形成した。

【0188】該SiO₂層表面と別に用意した500nmのSiO₂層を形成した2枚のSi基板の表面とをそれぞれ重ね合わせ、接触させた後、600 $^{\circ}\text{C}$ -2時間の熱処理をし、貼り合わせをおこなった。

【0189】ウェハ端面に多孔質層を表出させ、多孔質Siに水等の液体をしみ込ませた後、貼り合わせウェハ全体を加熱あるいは冷却したところ、液体の膨張等により多孔質Si層が破壊しウェハは二分割され、多孔質Siが表出した。

【0190】その後、多孔質Si層を49%弗酸と30%過酸化水素水との混合液(1:5)で攪はんしながら選択エッチングする。単結晶Siはエッチングされずに残り、単結晶Siをエッチ・ストップの材料として、多孔質Siは選択エッチングされ完全に除去された。

【0191】非多孔質Si単結晶の該エッチング液に対するエッチング速度は、極めて低く、多孔質層のエッチング速度との選択比は十の五乗以上にも達し、非多孔質層におけるエッチング量(数十オングストローム程度)は実用上無視できる膜厚減少である。

【0192】すなわち、Si酸化膜上に1 μ mの厚みを持った単結晶Si層が2枚同時に形成できた。多孔質S

iの選択エッチングによっても単結晶Si層には何ら変化はなかった。

【0193】透過電子顕微鏡による断面観察の結果、Si層には新たな結晶欠陥は導入されておらず、良好な結晶性が維持されていることが確認された。

【0194】エピタキシャルSi層表面に酸化膜を形成しなくても同様の結果が得られた。

【0195】第1のSi単結晶基板は残留多孔質Siを除去して、表面を水素処理して平坦化した後、再度第1のSi単結晶基板として使用した。

【0196】(実施例11) 625 μ mの厚みを持った比抵抗0.01 $\Omega \cdot \text{cm}$ のP型あるいはN型の5インチ径の第1の(100)単結晶Si基板を、HF溶液中において陽極化成を行った。

【0197】陽極化成条件は以下のとおりであった。

【0198】電流密度: 7 (mA $\cdot \text{cm}^{-2}$)

陽極化成溶液: HF:H₂O:C₂H₅OH=1:1:1

時間: 4 (分)

多孔質Siの厚み: 3 (μ m)

Porosity: 15 (%)

さらに

電流密度: 30 (mA $\cdot \text{cm}^{-2}$)

陽極化成溶液: HF:H₂O:C₂H₅OH=1:3:2

時間: 3 (分)

多孔質Siの厚み: 10 (μ m)

Porosity: 45 (%)

この基板を酸素雰囲気中400 $^{\circ}\text{C}$ で1時間酸化した。この酸化により多孔質Siの孔の内壁は熱酸化膜で覆われた。多孔質Si上にCVD法により単結晶Siを0.3 μ mエピタキシャル成長した。成長条件は以下の通りである。

【0199】ソースガス: SiH₄

キャリアーガス: H₂

温度: 850 $^{\circ}\text{C}$

圧力: 1 $\times 10^{-2}$ Torr

成長速度: 3.3nm/sec

さらに、このエピタキシャルSi層表面に熱酸化により100nmのSiO₂層を形成した。

【0200】該SiO₂層表面と別に用意した500nmのSiO₂層を形成したSi基板の表面とを重ね合わせ、接触させた後、700 $^{\circ}\text{C}$ -2時間の熱処理をし、貼り合わせをおこなった。

【0201】第1(あるいは第2)の基板に対して第2(あるいは第1)の基板に水平方向に力を加えたところ多孔質Si層は剪断応力に耐えきれず破壊しウェハは二分割され、多孔質Siが表出した。

【0202】その後、多孔質Si層をHF/HNO₃/CH₃COOH系のエッチング液で選択エッチングす

る。多孔質Siは選択エッチングされ完全に除去された。

【0203】非多孔質Si単結晶の該エッチング液にたいするエッチング速度は、極めて低く、非多孔質層におけるエッチング量は実用上無視できる膜厚減少である。

【0204】すなわち、Si酸化膜上に1μmの厚みを持った単結晶Si層が形成できた。多孔質Siの選択エッチングによっても単結晶Si層には何ら変化はなかった。

【0205】透過電子顕微鏡による断面観察の結果、Si層には新たな結晶欠陥は導入されておらず、良好な結晶性が維持されていることが確認された。

【0206】エピタキシャルSi層表面に酸化膜を形成しなくても同様の結果が得られた。

【0207】第1のSi単結晶基板は残留多孔質Siを除去して、再度第1のSi単結晶基板として使用した。

【0208】(実施例12) 625μmの厚みを持った比抵抗0.01Ω・cmのP型あるいはN型の5インチ径の第1の(100)単結晶Si基板を、HF溶液中において陽極化成を行った。

【0209】陽極化成条件は以下のとおりであった。

【0210】電流密度: 7 (mA・cm⁻²)

陽極化成溶液: HF:H₂O:C₂H₅OH=1:1:1

時間: 4 (分)

多孔質Siの厚み: 3 (μm)

Porosity: 15 (%)

さらに

電流密度: 30 (mA・cm⁻²)

陽極化成溶液: HF:H₂O:C₂H₅OH=1:3:2

時間: 3 (分)

多孔質Siの厚み: 10 (μm)

Porosity: 45 (%)

この基板を酸素雰囲気中400℃で1時間酸化した。この酸化により多孔質Siの孔の内壁は熱酸化膜で覆われた。多孔質Si上にCVD法により単結晶Siを0.3μmエピタキシャル成長した。成長条件は以下の通りである。

【0211】ソースガス: SiH₄

キャリアガス: H₂

温度: 850℃

圧力: 1×10⁻²Torr

成長速度: 3.3nm/sec

さらに、このエピタキシャルSi層表面に熱酸化により100nmのSiO₂層を形成した。

【0212】該SiO₂層表面と別に用意した500nmのSiO₂層を形成したSi基板の表面とを重ね合わせ、接触させた後、700℃-2時間の熱処理をし、貼り合わせをおこなった。

【0213】ウェハ端面に多孔質層を表出させ、多孔質Siの選択エッチング液により端面から多孔質Si層をエッチングしたところウェハは二分割された。

【0214】その後、多孔質Si層をHF/HNO₃/CH₃COOH系のエッチング液で選択エッチングする。多孔質Siは選択エッチングされ完全に除去された。

【0215】非多孔質Si単結晶の該エッチング液にたいするエッチング速度は、極めて低く、非多孔質層におけるエッチング量は実用上無視できる膜厚減少である。

【0216】すなわち、Si酸化膜上に1μmの厚みを持った単結晶Si層が形成できた。多孔質Siの選択エッチングによっても単結晶Si層には何ら変化はなかった。

【0217】透過電子顕微鏡による断面観察の結果、Si層には新たな結晶欠陥は導入されておらず、良好な結晶性が維持されていることが確認された。

【0218】エピタキシャルSi層表面に酸化膜を形成しなくても同様の結果が得られた。

【0219】第1のSi単結晶基板は残留多孔質Siを除去して、再度第1のSi単結晶基板として使用した。

【0220】

【発明の効果】以上説明したように、本発明によれば、貼り合わせて構成された基体を多孔質層で分離し、非多孔質単結晶半導体層が配された第2の基体上の多孔質層を除去することにより、高品質な非多孔質単結晶半導体層が配された半導体基体を形成できる。

【0221】これに加えて、貼り合わせて構成された基体を多孔質層で分離し、第1の基体を構成する多孔質層を除去することにより、多孔質層を除去した第1の基体を半導体基体作製に再利用することができるため、半導体基体の生産性の向上、低コスト化が更に図れる。

【0222】また、本発明によれば、透明基板(光透過性基板)をはじめとする基板上に結晶性が単結晶ウェハー並に優れたSi等の単結晶層あるいは化合物半導体単結晶層を得るうえで、生産性、均一性、制御性、コストの面において卓越した半導体基板の作製方法を提案することができる。

【0223】また、本発明によれば、SOI構造の大規模集積回路を作製する際にも、高価なSOSや、SIMOXの代替足り得る半導体基板の作製方法を提案することができる。

【0224】また、本発明によれば、多孔質層を介して基体を2つ以上に分離することができ、分離後の一方の基体は、残留多孔質を除去した後、半導体基板として使用可能であり、他方の基体は、残留多孔質を除去した後、再度、半導体基板の作製に利用することができる。

【0225】また、本発明によれば、基体の両面に多孔質層および非多孔質単結晶層を形成し、該単結晶層を挟むように2枚の別の基体を貼り合わせた後、前記多孔質

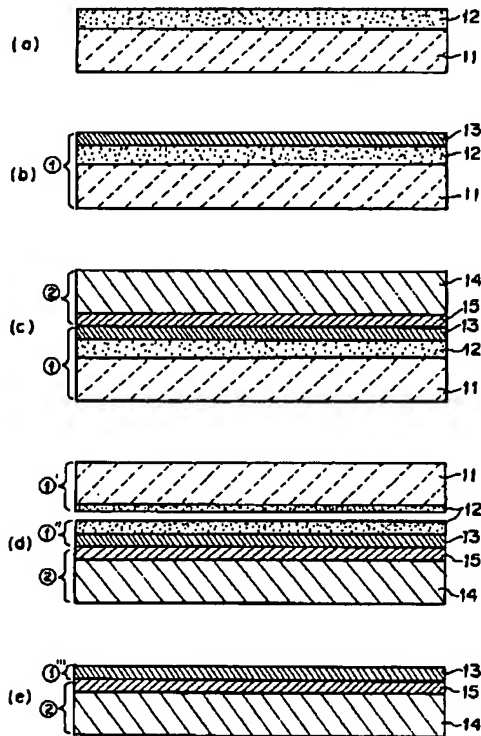
層で基体を分離することにより同時に 2 枚の半導体基板を作製することができる。

【0226】すなわち、本発明によれば、経済性に優れて、大面積に渡り均一平坦な、極めて優れた結晶性を有する単結晶基板を用いて、表面に形成された半導体層あるいは化合物半導体活性層を残して、その片面から該活性層までを取り去り、絶縁物上に欠陥の著しく少ない単結晶層あるいは化合物半導体結晶層を得る半導体基板の作製方法を提供することができる。

【0227】また、透明基板（光透過性基板）上に結晶性が単結晶ウェハ一並に優れた Si あるいは化合物半導体単結晶層を得るうえで、生産性、均一性、制御性、コストの面において卓越した半導体基板の作製方法を得ることができる。

【0228】また、SOI 構造の大規模集積回路を作製する際にも、高価な SOS や、SIMOX の代替足り得る半導体基板の作製方法を得ることができる。

【図 1】



【図面の簡単な説明】

【図 1】本発明の方法の 1 例を説明するための模式的断面図である。

【図 2】本発明の方法の 1 例を説明するための模式的断面図である。

【図 3】本発明の方法の 1 例を説明するための模式的断面図である。

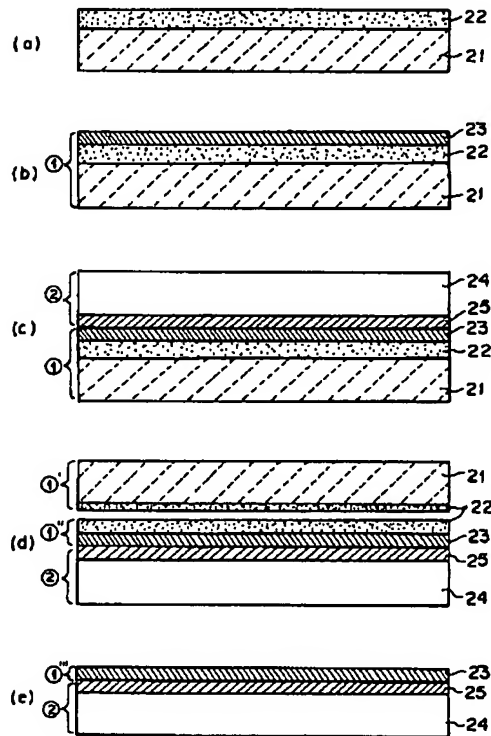
【図 4】本発明の方法の 1 例を説明するための模式的断面図である。

【図 5】本発明の方法の 1 例を説明するための模式的断面図である。

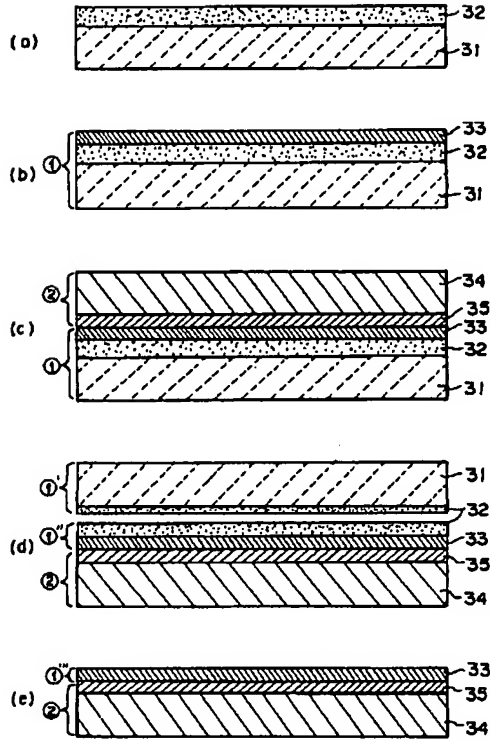
【符号の説明】

- 11 Si 単結晶基板
- 12 多孔質 Si 層
- 13 非多孔質単結晶 Si 層
- 14 Si 支持基板
- 15 絶縁層

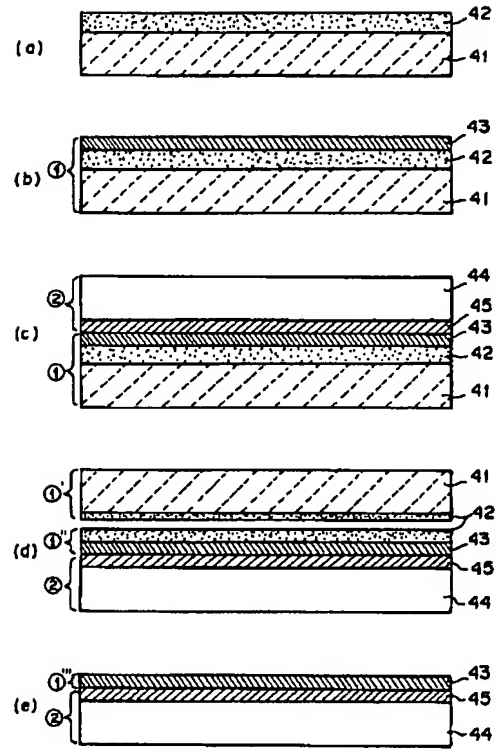
【図 2】



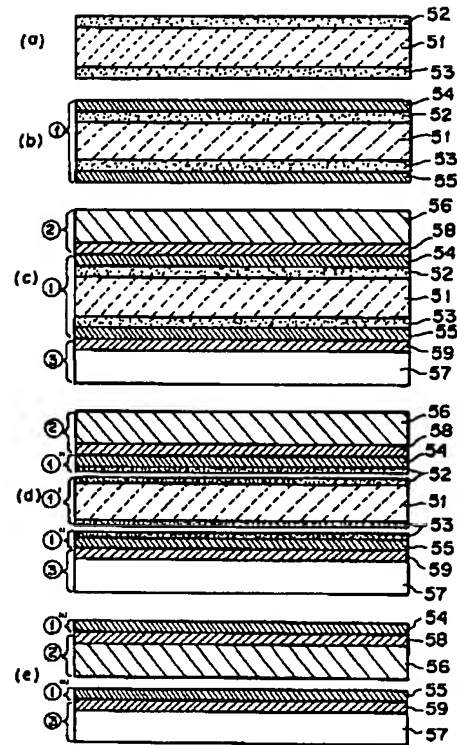
【図 3】



【図 4】



【図 5】



フロントページの続き

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